JUNE 14, 1984

IC MAKERS TARGET GALLIUM ARSENIDE FOR COMMERCIALIZATION/ 101

Novel architecture adds features to 256-K C-MOS dynamic RAM/138

Flexible programming language simplifies robot control/156

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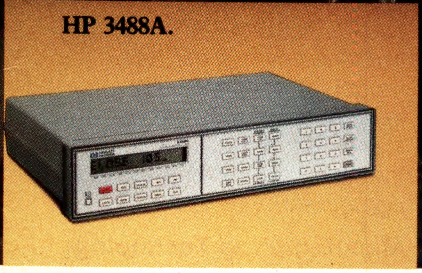

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New Products

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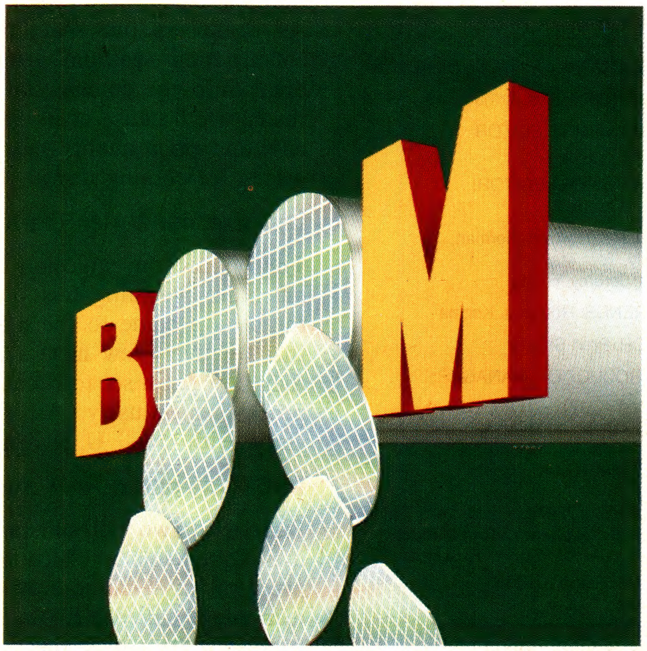
Cover illustration by David Myers



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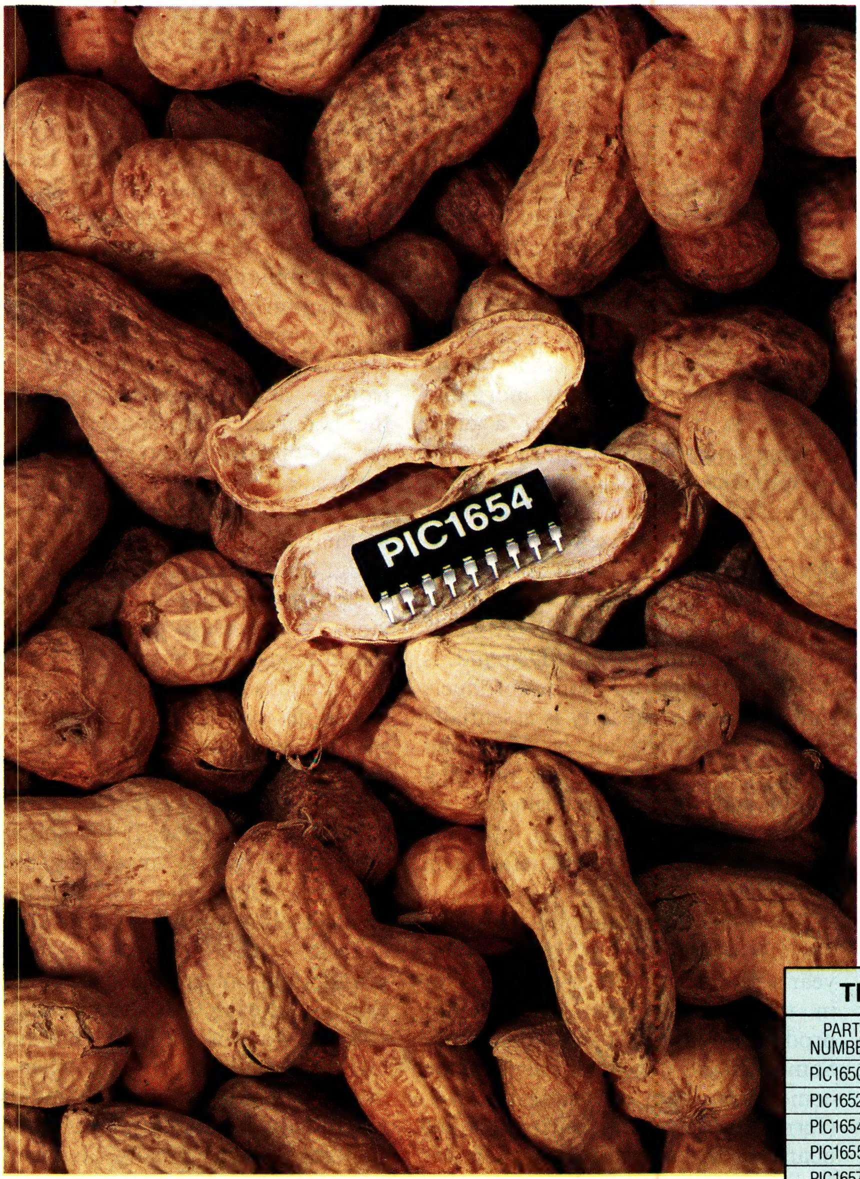
In a nutshell: The Smallest 8-Bit Microcomputer



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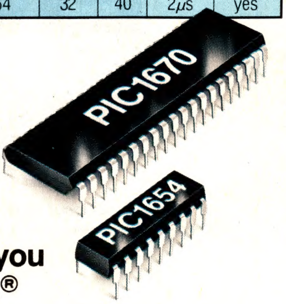
PIC1652	256 x 12	32	12	18	2μs	no
PIC1654	512 x 12	32	12	18	2μs	no
PIC1655A	512 x 12	32	20	28	4μs	no
PIC1657	512 x 12	32	20	28	2μs	no
PIC16C58	512 x 12	32	20	28	4μs	no
PIC1670	1024 x 13	64	32	40	2μs	yes
PIC1672	2048 x 13	64	32	40	2μs	yes



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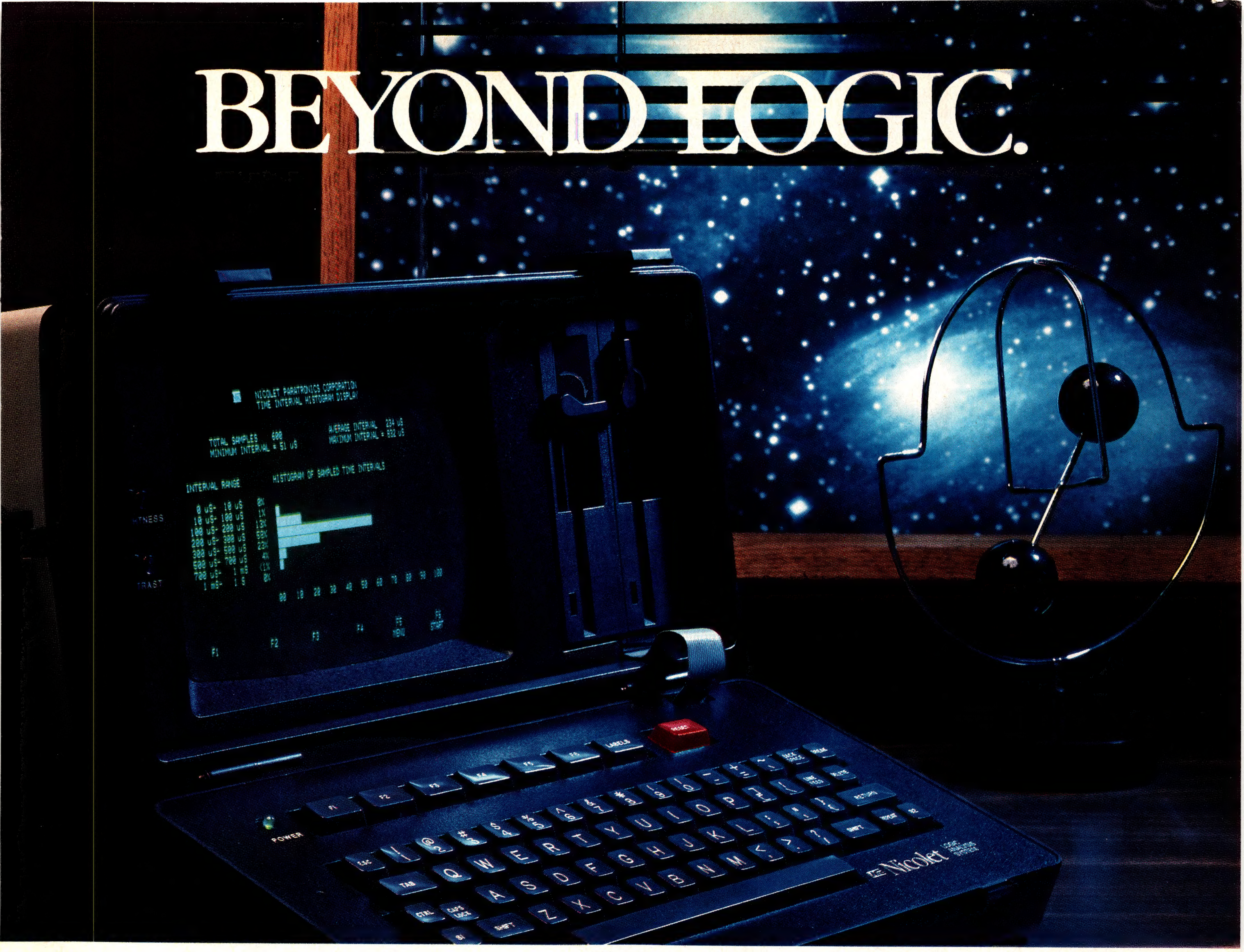
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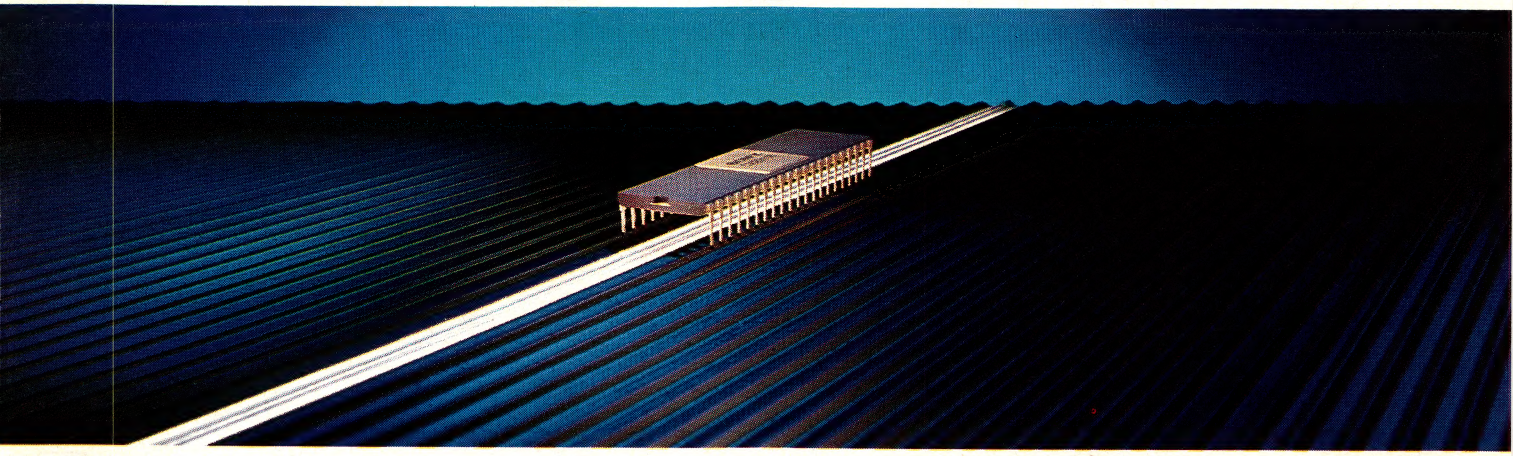
8-bit analog to digital at 100MHz.



You are looking at one of the most significant breakthroughs in digital technology : the amazing Sony CX20116 single-chip analog to digital converter. Requiring a mere 1,200 mW, this remarkable 8-bit processor accepts signal bandwidth up to 40MHz and works at a clock speed of 100MHz, fast enough for the most demanding video requirements. Fast enough to realize in reality what was once only a theoretical possibility. Extraordinary sampling rates and high resolution are possible. And most important of all, Sony offers it now. At one time, Sony's advanced integrated circuit technology was limited to Sony's own product development engineers. Now you can have this same high-quality capability for your own products. The Sony 100MHz analog to digital converter is the first in a series of leading-edge digital signal processing microelectronic products that Sony will be offering. You can be certain that each of them will be a major advance in the state of the art. That's what you'd expect from Sony.

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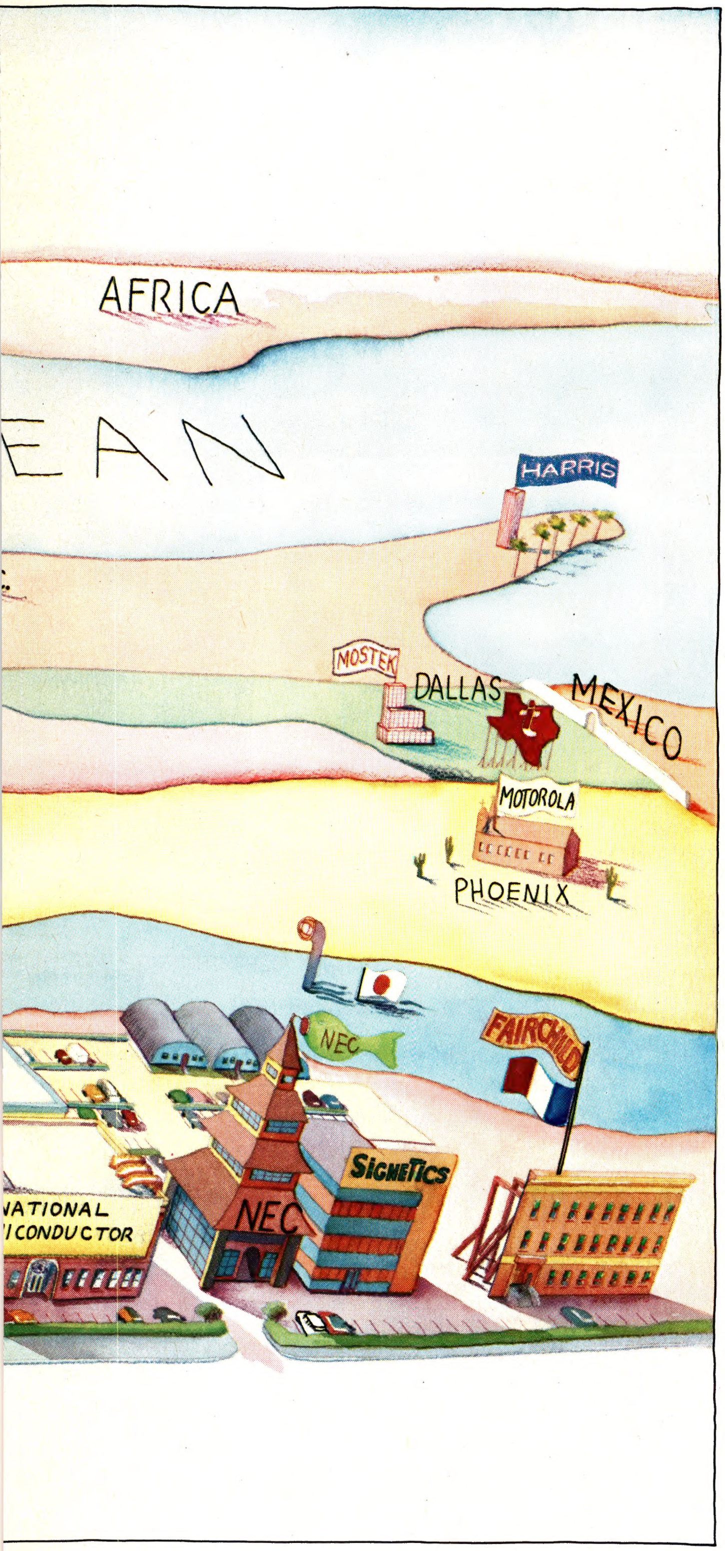

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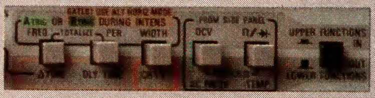

For the same effort previously required just to display the waveform you can obtain digital readout of frequency, period, width, totalized events, delay time and Δ-time to accuracies of 0.001%.

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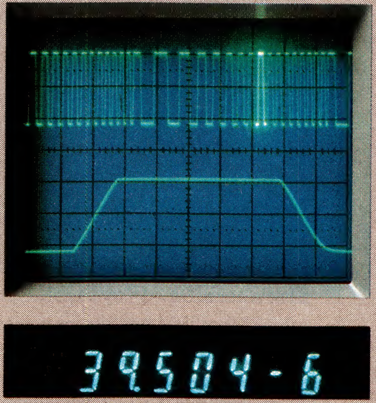
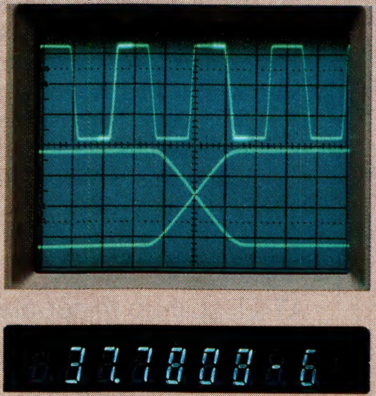
Left top: Ch 1 true RMS & DC volts measurements. Made easily at the probe tip. (The 2236 adjusts automatically to 1X or 10X probes.) The 2236 includes relative reference capability for subtracting offsets.

Left bottom: Gated frequency measurement. Intensified zone brackets the period of interest by means of the delayed sweep, allowing easy frequency measurement on any specified portion of the waveform.



Gated width measurement. Pulse of interest is selected with the intensified zone. Both width and period measurements are made with up to 10 ps resolution.



Delta time measurement. Time between two intensified zones on the A sweep is measured with up to 50 ps accuracy.

You can obtain scope, counter and DMM input simultaneously through a single probe. The same probe is used to provide input for the 2236 CRT display and the digital measurement system resulting in easy set-up, greater measurement confidence and reduced circuit loading. You can make direct digital measurement of dc volts and ac coupled true RMS volts through the Ch 1 input.

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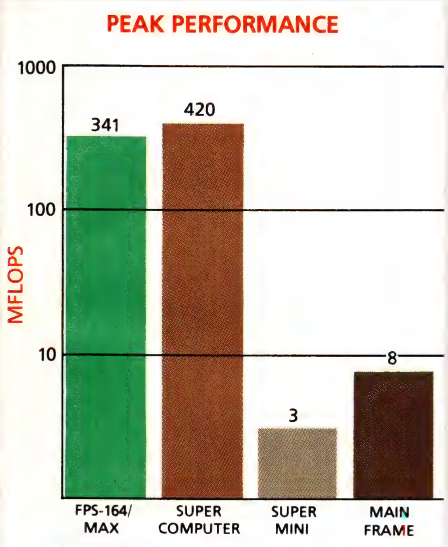

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Number of Arithmetic Pipelines	63
Number of Independent Processors	1
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Main Memory Capacity	7 MWords
Disk Subsystem Capacity	3 Gbytes
Word Size	64 bits +8-bit error correction
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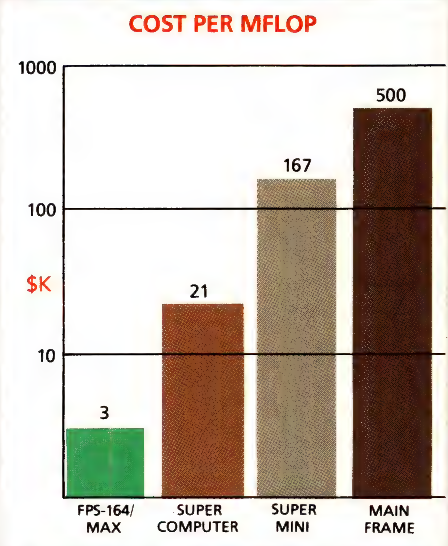

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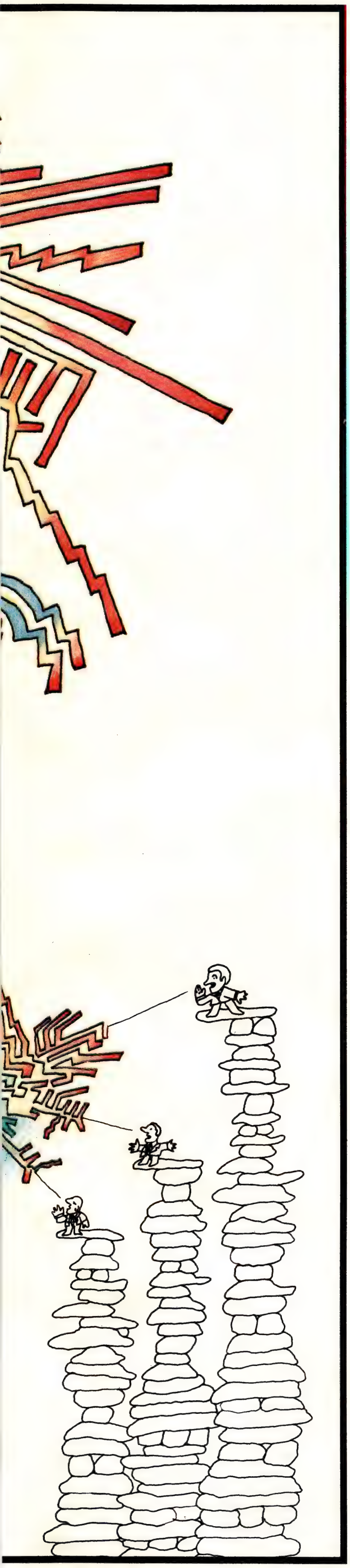

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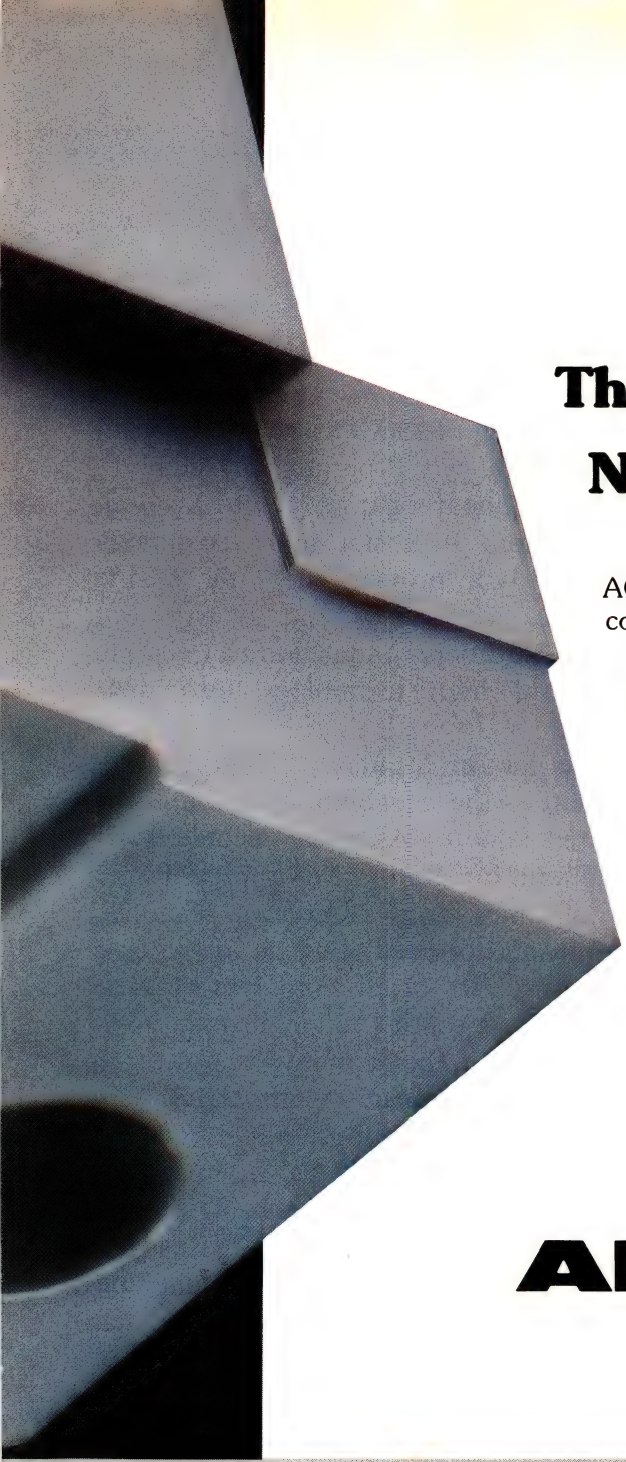

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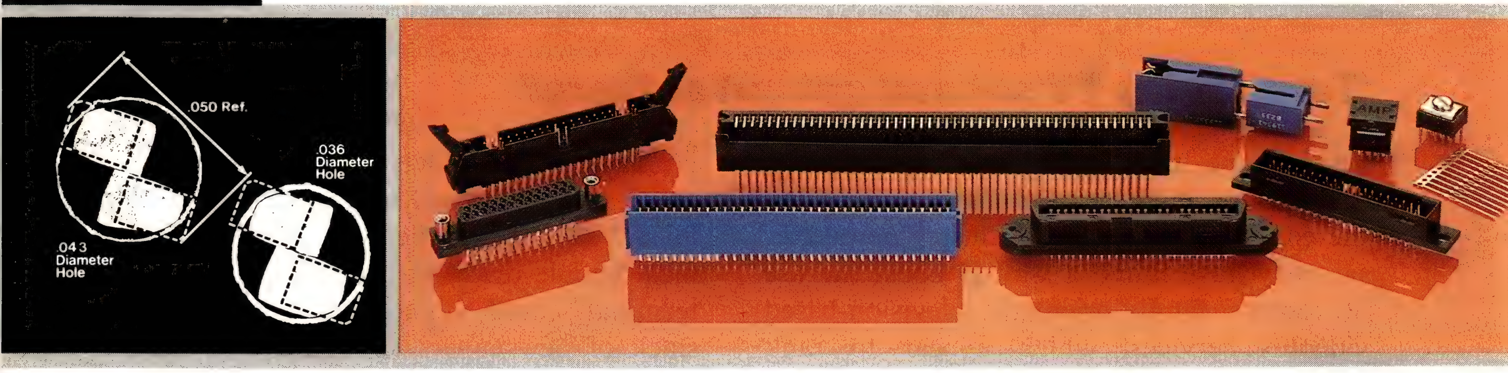

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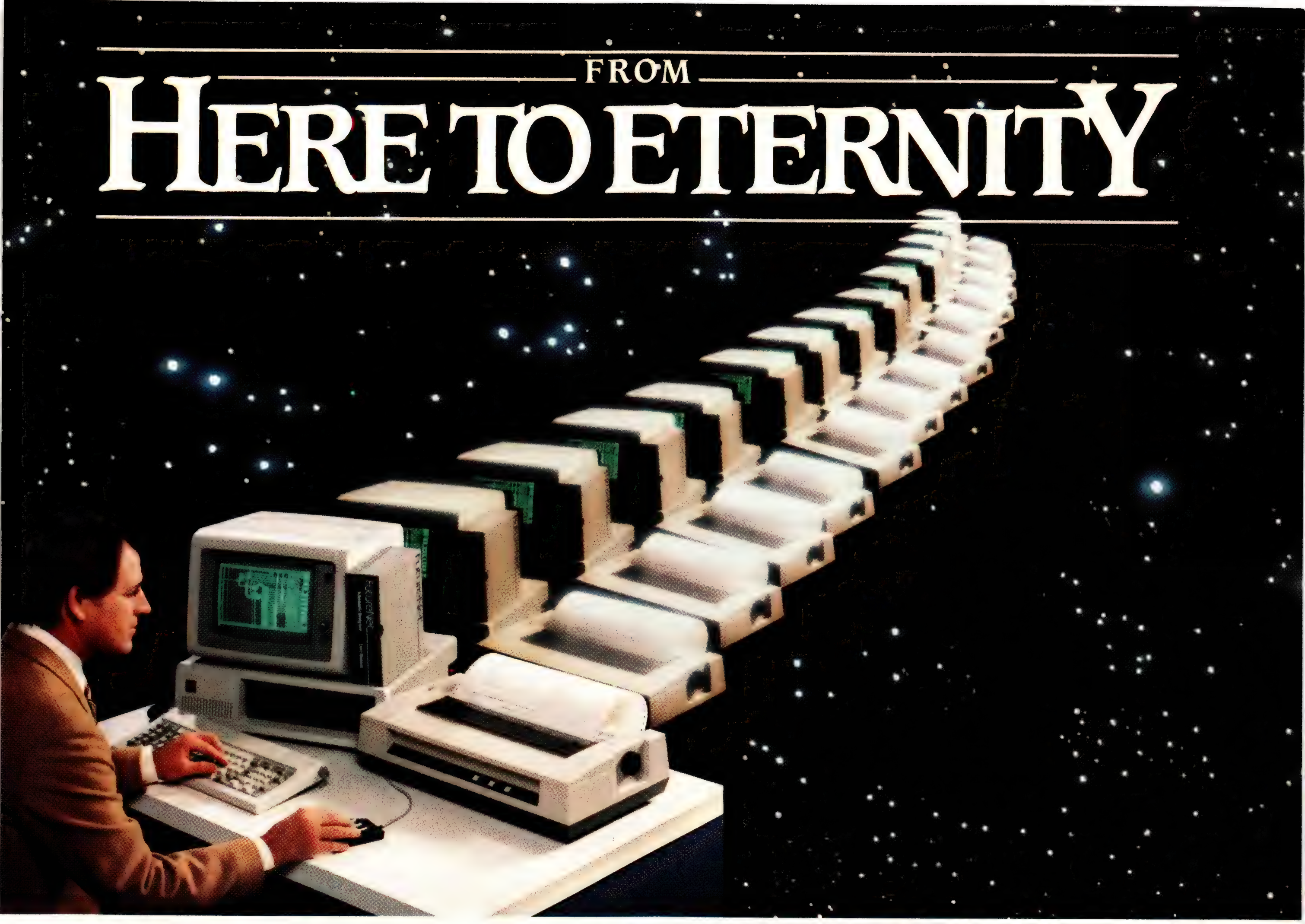

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Now, DASH-1 is equally capable of handling the future. New interfaces for the most complex CAD systems are now on-line. Classic examples are TEGAS and SCICARDS. Direct connection to DEC, IBM and other computers is a snap. And as new advanced CAD systems unfold, DASH-1's versatility defies obsolescence.

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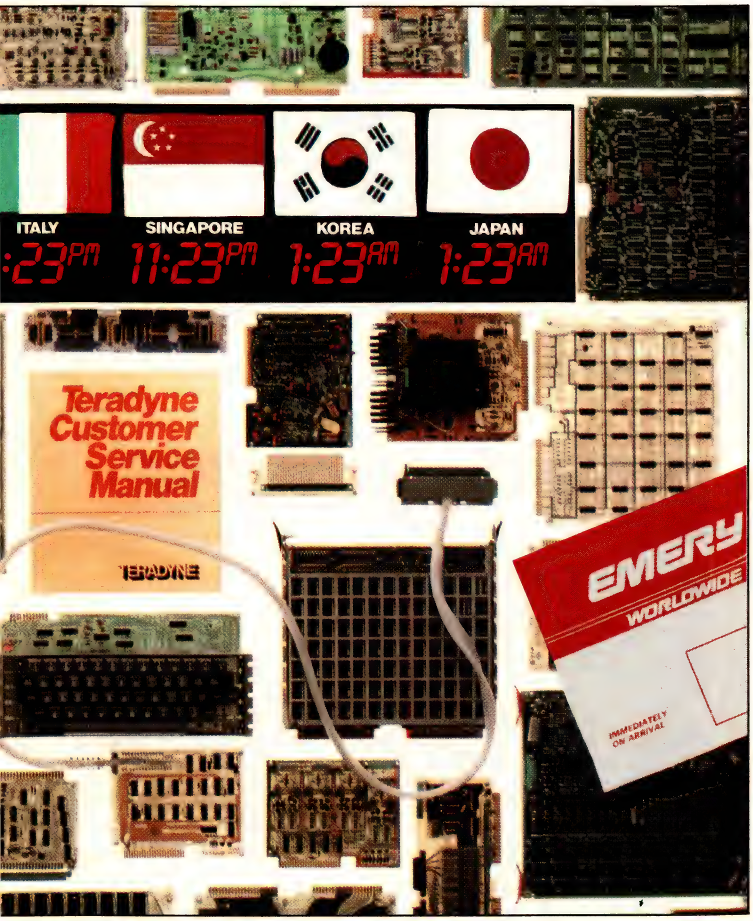

But not to worry. We can be absolutely candid about this for two reasons. First, we know that within any reasonable framework, Teradyne equipment performs superbly.

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TERADYNE

We measure quality

Circle 29 on reader service card

Design News

G

High-speed, high-voltage Ultrafasts also low cost.

Sporting 60 ns maximum reverse recovery times, the new MUR1530-1560 Ultrafast rectifiers are ideal for high-voltage designs barrier rectifiers can't quite reach. Reverse voltage is spec'd to 600 V for these popular TO-220 units which offer maximum 1.2-1.5 V_F characteristics.

High-current is another plus: 15 A at 145°/150°C for big-power jobs in switching power supplies, inverters, and free-wheeling diodes. Current derating is spec'd at both case and ambient temperatures for a clear performance picture.

Best of all, price...just $1.90 to $2.25, 100-up, for the series, proof once again Motorola fast-rectifier leadership offers more for less.

H

High-voltage deflection brightens with discretes, Darlingtons.

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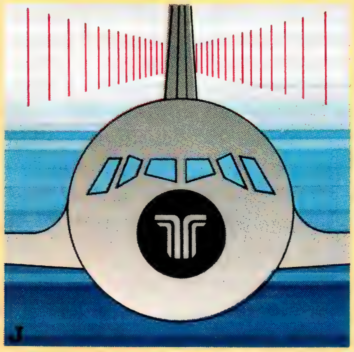
The BU806/807, 8 A, 150 and 200 V_{CEO}, 330 and 440 V_{CEV} Darlingtons in TO-220 fit right into cost-conscious applications in PCs and smaller-sized CRTs. They're fast, with 1 μs max crossover time and low-sat-efficient at 1.5 $V_{CE(sat)}$ max. Equally significant are internal damper and speed-up diodes for cost and space-efficient real estate. $1.55 and $1.65, 100-up.

The 8 A, 1,500 V MJI2005D has a V_F-spec'd, cost-reducing CE diode too, minimizing oscillation and breakdown, plus a 20 A @ 400 V SOA specially adaptable to flyback clamps and larger screens needing that inherent Motorola ruggedness. Switching time is typically 0.4 μs @ 5 A; glassivated junctions ensure reliability. $4.30, 100-up.



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Higher gain, stability in avionics with TMOS™ RF

TMOS power technology isn't limited to low-frequency with Motorola.

We've adapted its superiority to high-frequency devices, too, this time in the MRF163 MOSFET for the 225-400 MHz Avionics band.

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It's suitable for Class A or Class C applications and priced at $18, 100-up.

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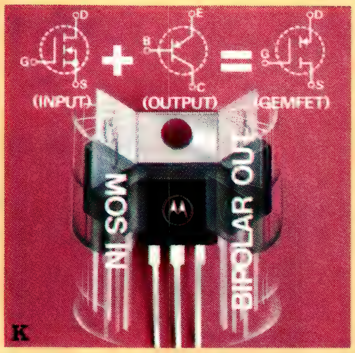

K

GEMFET™ power MOSFETs cut conduction losses 6 to 10 times.

What may be the next generation of power MOSFETs is already making inroads into new design.

The MGM/MGP20N45 and MGM/MGP20N50 are 20 A, 450 and 500 V GEMFETs (Gain-Enhanced MOSFETs) offer "on" resistance of only 0.27Ω. Equivalent power MOSFET devices spec out around 1.5Ω.

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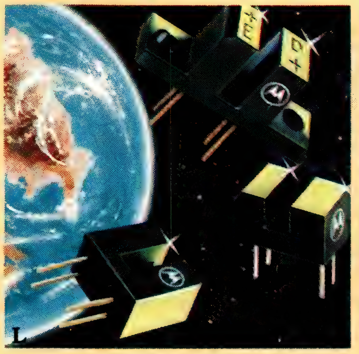
These initial units are available in TO-204AA (formerly TO-3) and plastic TO-220AB packages and are intended for DC and low-frequency applications such as variable voltage, variable frequency, motor control and inverter designs.



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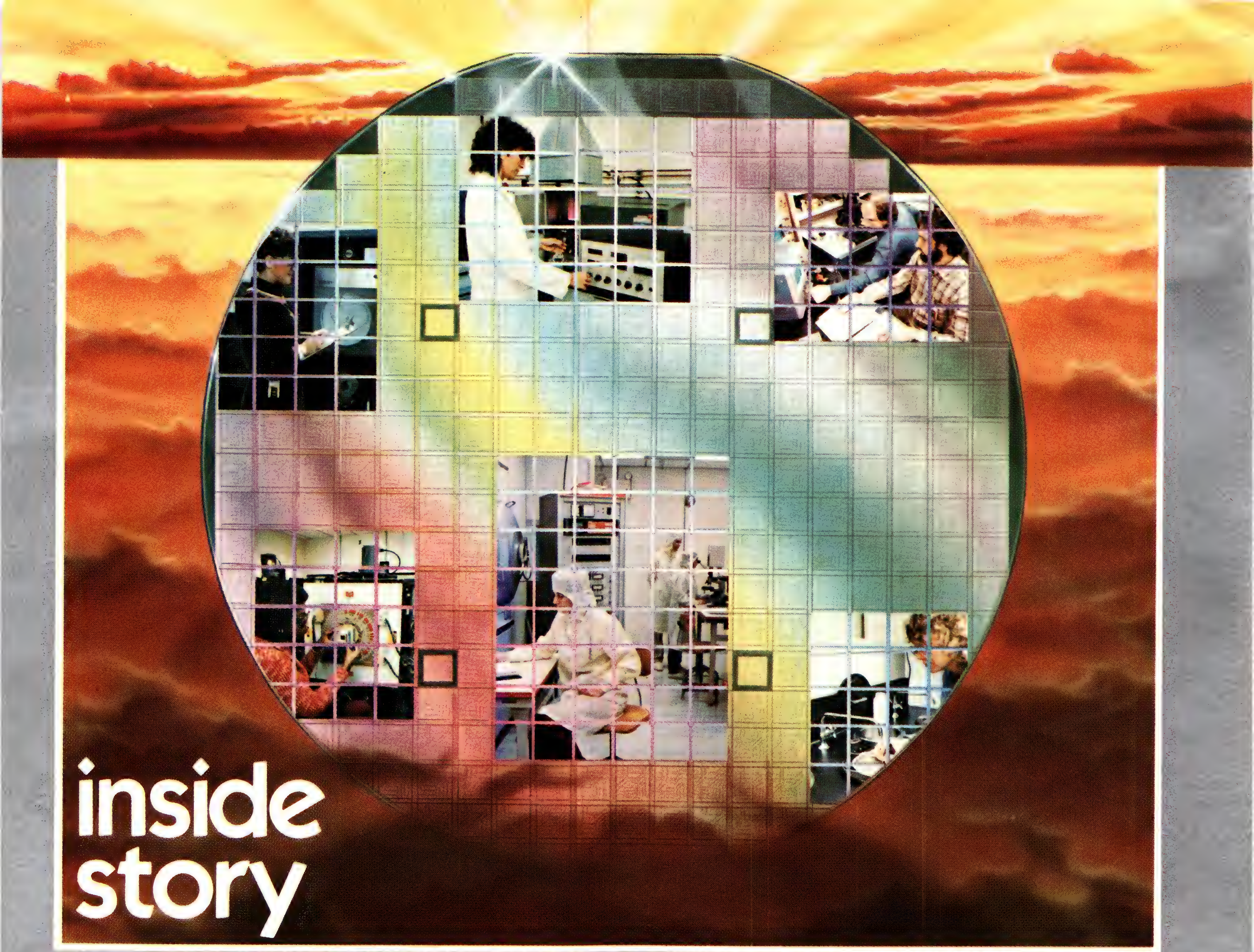

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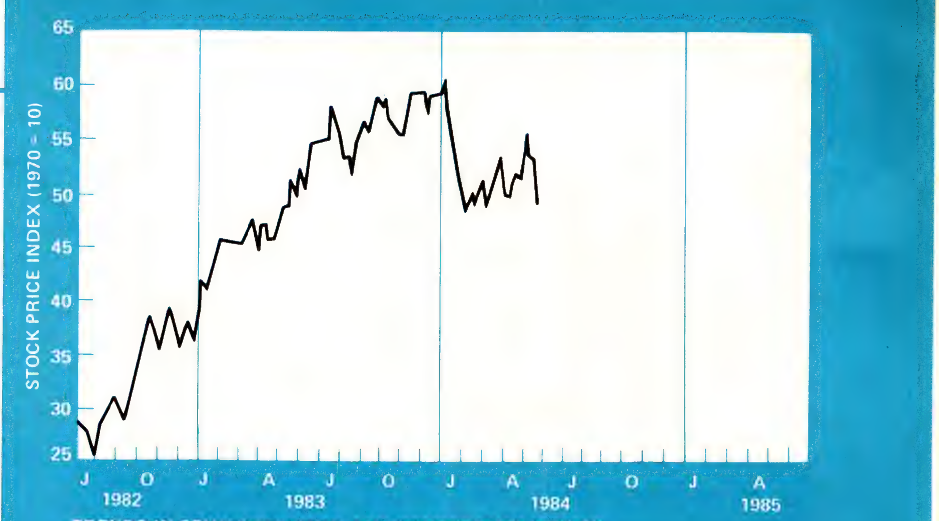

TRENDS IN SEMICONDUCTOR AND COMPONENTS STOCKS

SOURCE: STANDARD & POOR'S CORP.

Where is the U. S. economy going in the months ahead? One possible answer comes from Robert A. Gough, senior vice president and senior economist for Data Resources Inc., an econometric forecasting firm in Lexington, Mass. He argues that growth in the U. S. economy will slow to the 4%-to-5% range over the next few months but will then face "a hard landing" late this year or early next. There are several positive factors now influencing the economy, he says. One is the strength of the U. S. consumer's financial condition, with low household debt, strong income, and confidence in the economy. Another is inventory levels at manufacturing companies which, despite recent buildups, are not out of line with levels reached in other recovery periods. In addition, the rise in inflation is still moderate. Gough says that two presently neutral factors—the housing and the car markets—could turn either positive or negative. "There is tremendous stability in the housing market now," he says, with no big surge and no big drop in buying. As for car sales, they are "not bad but not particularly good."

The two big risks are the condition of corporate balance sheets, which he described as "very, very bad," and the Federal deficit. Debt-to-equity ratios are too high at too many firms, Gough argues, which means that they will have trouble financing capital spending. A package passed by Congress to alleviate the deficit in future years "only holds the deficit where it is," Gough says, at about $190 billion by 1986, instead of helping to eliminate it altogether. If nothing further is done to cut the deficit, the economy could stumble and fall into another 6-to-8-month recession.

Company financings. . . . *Protocom Devices*, a Stamford, Conn., maker of data-communications equipment, has received $4.4 million from the Port Authority of New York and New Jersey. The firm will use the funds to develop manufacturing facilities in the South Bronx. . . . *IDE Associates Inc.*, Bedford, Mass., which makes peripheral equipment for the IBM Corp. Personal Computer, received $3.25 million from a third round of financing. . . . *Aseco Corp.*, Marlboro, Mass., has obtained $980,000 in venture capital. The firm is developing package-handling equipment for new surface-mounted integrated circuits and chip-carriers. . . . A new round of financing brought an investment of $1.5 million in venture capital to *Microlink Corp.*, Carmel, Ind., which develops STD-bus products.

–Robert J. Kozma

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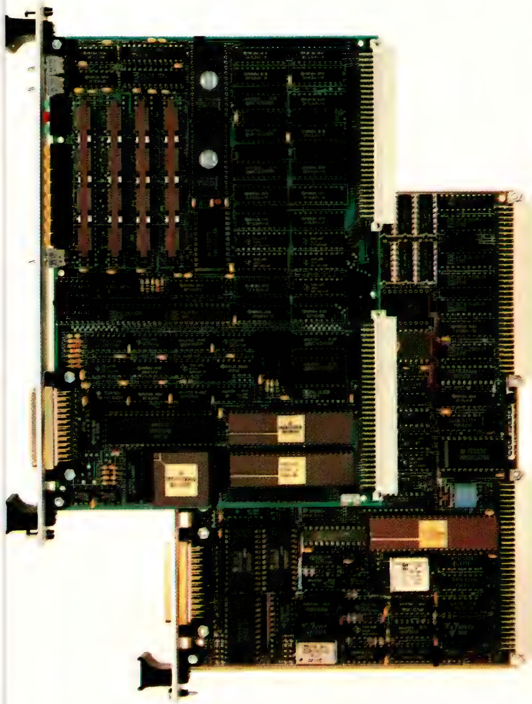

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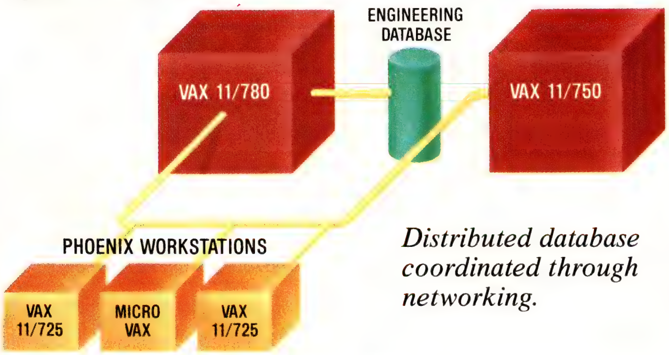

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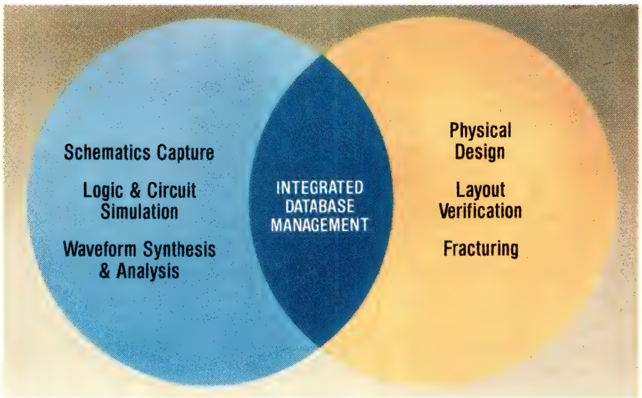
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Circle 39 on reader service card

Electronics newsletter

Datapoint goes to open systems . . .

In a major departure from its policy of making and selling closed proprietary systems, Datapoint Corp., the San Antonio, Texas, office-automation supplier, announced a bevy of new products last week that makes it an open-systems supplier as well. The major announcement is the first in a while from the company that pioneered local networking but ran into severe marketing and financial problems two years ago. **Included are products made by other companies as well as products running independent operating systems**—MS-DOS for starters. All Datapoint's products attach to its office-automation network, called ARC (Attached Resource Computing), which the company has now opened up to non-Datapoint equipment. Company president Edward P. Gistaro says that the opening-up of ARC "will include the IBM Personal Computer integrated directly into ARC in the future."

. . . and offers its own N-Gen-based computer

Datapoint has joined the swelling ranks of major companies (including Burroughs, NCR, Gould, and Mohawk) offering a product based on the N-Gen work station made by Convergent Technologies, of Santa Clara, Calif. The Datapoint version, called the Vista PC, has a 13-in. color monitor, runs MS-DOS, and will have an ARCnet connection by the end of the year. **Also announced were the Vista-Station 84, an applications processor based on the Intel 80286** processor, and a companion terminal, the Vista-Station 82, which uses the 80186. Finally, the company unveiled a fiber-optic-link option for ARC and what it calls a fourth-generation windowing software package for the Vista work stations.

RCA and others put 8-mm video on hold

Following a flurry of hurried 8-mm-video prototype rollouts at last January's Las Vegas Consumer Electronics Show [*Electronics,* Jan. 26, p. 94], a calmer atmosphere surrounded the controversial new format at the summer edition of the show, last week in Chicago. As sales of conventional video-cassette recorders based on ½-in. tape continue to boom—this year's U. S. sales are projected to grow by 70%, to 7 million units—several manufacturers are putting their 8-mm plans on hold. For example, RCA Corp., which held private showings of a Hitachi-made 8-mm unit in January, now says it has no plans to market the system. **Technical problems have delayed the introduction of General Electric Co.'s 8-mm unit,** made by Matsushita. Only Eastman Kodak Co. and Polaroid Corp.—neither of which has a stake in the ½-in. business—are still announced 8-mm vendors. In Chicago, Polaroid, the newest entry, showed working models of a Toshiba-made one-piece camera-recorder and playback deck the company plans to market in the fourth quarter. Kodak, which touched off the January frenzy when it introduced an 8-mm player, says it is on schedule to market its Matsushita-made system in September.

Digital-disk players to appear in 1985 cars

With problems of size, heat, and vibration apparently overcome, digital audio disks will soon take to the road. Manufacturers at last week's Summer Consumer Electronics Show in Chicago were promising U. S. deliveries early next year on automobile players in the Compact Disc technology. For instance, the CDX-1 unit shown by Pioneer Electronics (USA) Inc. and set for January introduction features a modular design to

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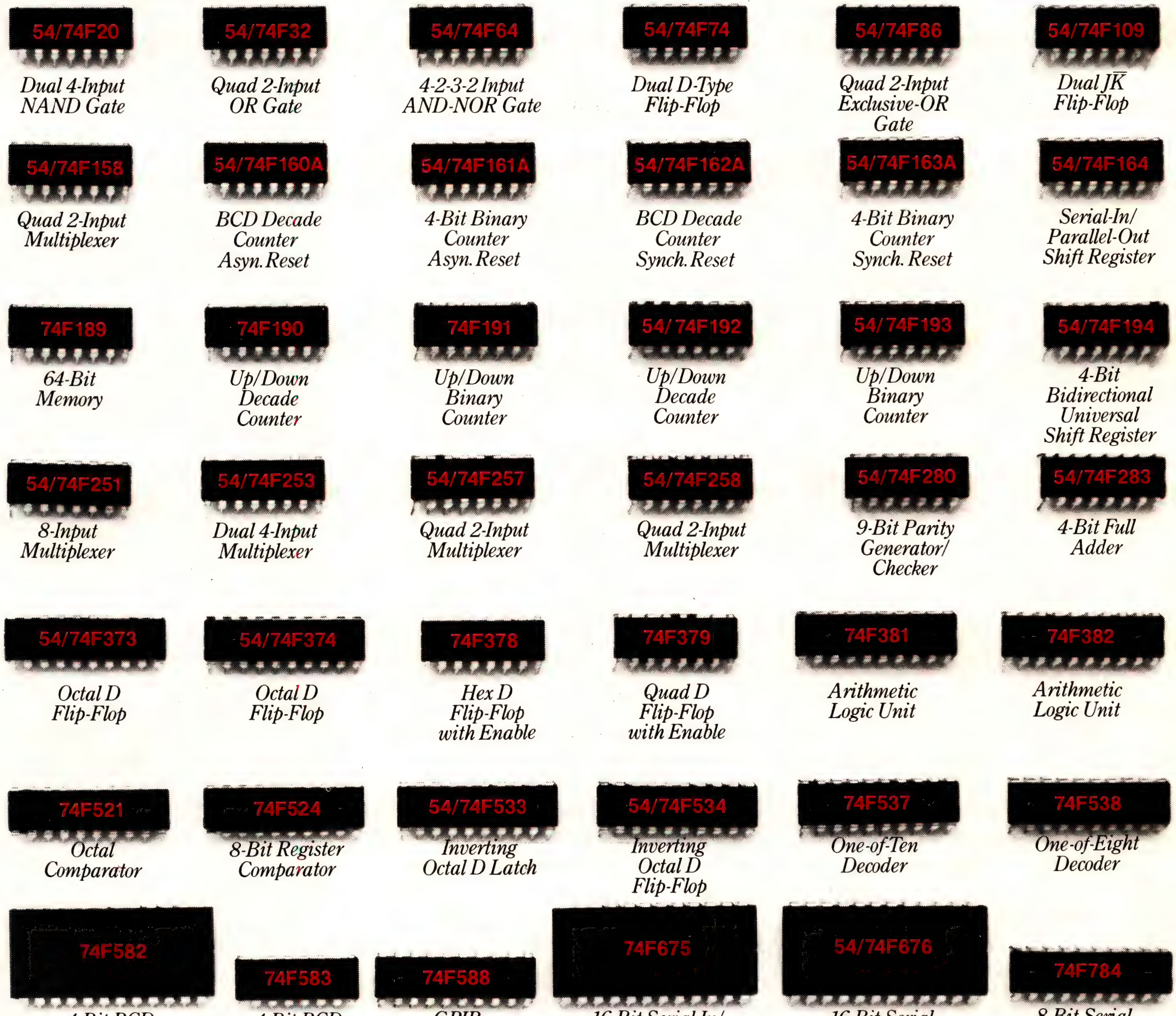
ANSWERS.



Part	Description
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54/74F32	Quad 2-Input OR Gate
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54/74F74	Dual D-Type Flip-Flop
54/74F86	Quad 2-Input Exclusive-OR Gate
54/74F109	Dual $J\overline{K}$ Flip-Flop
54/74F158	Quad 2-Input Multiplexer
54/74F160A	BCD Decade Counter Asyn. Reset
54/74F161A	4-Bit Binary Counter Asyn. Reset
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54/74F163A	4-Bit Binary Counter Synch. Reset
54/74F164	Serial-In/ Parallel-Out Shift Register
74F189	64-Bit Memory
74F190	Up/Down Decade Counter
74F191	Up/Down Binary Counter
54/74F192	Up/Down Decade Counter
54/74F193	Up/Down Binary Counter
54/74F194	4-Bit Bidirectional Universal Shift Register
54/74F251	8-Input Multiplexer
54/74F253	Dual 4-Input Multiplexer
54/74F257	Quad 2-Input Multiplexer
54/74F258	Quad 2-Input Multiplexer
54/74F280	9-Bit Parity Generator/ Checker
54/74F283	4-Bit Full Adder
54/74F373	Octal D Flip-Flop
54/74F374	Octal D Flip-Flop
74F378	Hex D Flip-Flop with Enable
74F379	Quad D Flip-Flop with Enable
74F381	Arithmetic Logic Unit
74F382	Arithmetic Logic Unit
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74F524	8-Bit Register Comparator
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Electronics report

Significant developments in technology and business

Early test generation is goal of software for work station

by J. Robert Lineback, Dallas bureau

New programs use data collected at beginning of design to automatically create series of tests

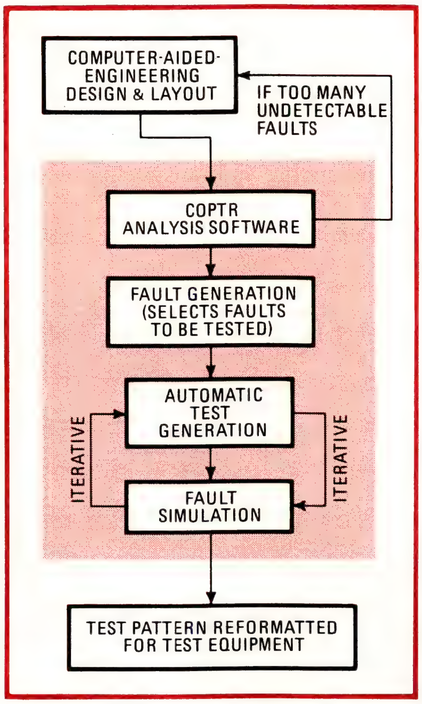
Vendors of engineering work stations are taking aim at a new breed of interactive design software that surpasses the capabilities of today's larger computers. The breakthrough, most agree, is likely to come when work stations integrate automatic-test-generation software into the early phases of design, giving engineers interactive tools that automatically generate tests as circuits are created. The goal, as it has been all along with large-system software, is to ensure the testability of complex chips and boards once they reach the production lines.

Already laying foundations for such computer-aided-design packages are General Electric Co.'s Calma Co., of Santa Clara, Calif., and Daisy Systems Corp., of Sunnyvale, Calif. At the Design Automation Conference in Albuquerque, N. M., June 25–27, both are planning to spotlight new test-pattern-generation programs that benefit from information collected in a data base during the design phase.

This new software initiative follows two years during which makers of microprocessor-based engineering work stations concentrated on duplicating the design-automation tools of minicomputers and mainframes.

Just as with its Tegas-5 software for larger computers, Calma's operation in Austin, Texas, is linking CAD on Apollo-based Tegastations with a sophisticated analysis software called Coptr, an acronym that stands for controllability-observability-predictability-testability report [*Electronics*, March 10, 1983, p. 120].

Coptr helps the test generator quickly navigate the network by passing along information about the logic paths in the layout. That, plus a new process that divides the entire circuit with small iterative steps of test-pattern generation and parallel fault grading, can give automatic-test-generation cycles five times faster than running Coptr-enhanced test generation alone, says Dave Niehaus, product manager of Tegastations.


COMPUTER-AIDED-ENGINEERING DESIGN & LAYOUT
IF TOO MANY UNDETECTABLE FAULTS
COPTR ANALYSIS SOFTWARE
FAULT GENERATION (SELECTS FAULTS TO BE TESTED)
AUTOMATIC TEST GENERATION
ITERATIVE
ITERATIVE
FAULT SIMULATION
TEST PATTERN REFORMATTED FOR TEST EQUIPMENT

Early warning. Steps in Calma's TCAT program are shown in tinted area. Automatic-test-generation and fault-simulation steps may employ iterative technology.

Even though test patterns are generated for a limited number of fault locations, each iterative loop can pick up untargeted faults as it works its way through the logic network. The data base keeps a record; the result is previously undetected faults, Niehaus adds.

The new computer-aided test package—dubbed TCAT—is part of the Tegastation release 3.0, to be introduced at the design show. The TCAT option will be available for delivery in October and sell for $10,000. The basic Calma Tegastations cost as little as $54,000 for 70 megabytes of hard-disk and 1.5 megabytes of main memory.

New data base. A key performance enhancement to the tandem of Coptr and automatic test generation is a reoriented data base. It logs detected, undetected, and undetectable fault locations in a single random-access master fault file, explains Niehaus. Since Coptr identifies faults that will never be detected by tests, automatic test generation and fault-grading programs will not waste time on untestable portions of the design.

TCAT is also being implemented in Tegas-5 software for minicomputers. However, it is only the beginning for Calma, which is now in the early development of a full-function interactive-test work station. Portions of the package, such as interactive fault grading networked to other work stations, will allow circuit engineers to introduce real-time test sizes and coverages as designs evolve.

Also at the show, Daisy plans to highlight its new test-pattern-generation tools, which create vectors for serial fault simulation on the Mega-Logician hardware accelerator en-

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SENIOR AND INTERMEDIATE GRADES

Familiarity with analysis of linear bipolar IC's (CMOS helpful). Will determine impact of design process on yield, sensitivity analysis and release of products to production, characterization of parts.

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Requires sold technical background in all phases of semiconductor manufacturing. Must be able to review engineering change orders, RFQs, vendor surveys and QA procedures. Will interact with customers and vendors.

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SENIOR AND INTERMEDIATE GRADES

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Candidates must be familiar with linear bipolar IC design and/or MOS IC design cycle from concept—determining specifications, doing computer simulation, breadboarding of circuit mask design, characterization of parts, analysis of yield—to release to preproduction/production.

SENIOR DESIGN ENGINEER (Telecommunications Group)

Knowledge of MOS design, PCM transmission techniques or data communication circuits.

SENIOR DESIGN ENGINEER (MOS Linear IC Group)

Requirements include knowledge of CMOS logic design, analog circuit blocks or switch capacitor filters.

DESIGN ENGINEERS (Linear Semi-Custom Group)

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Knowledge of a wide range of analog circuits required and the ability to operate in a dynamic environment. Interaction with customers. Familiarity with semi-custom design environment and techniques necessary.

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(Bipolar and/or MOS IC Groups)

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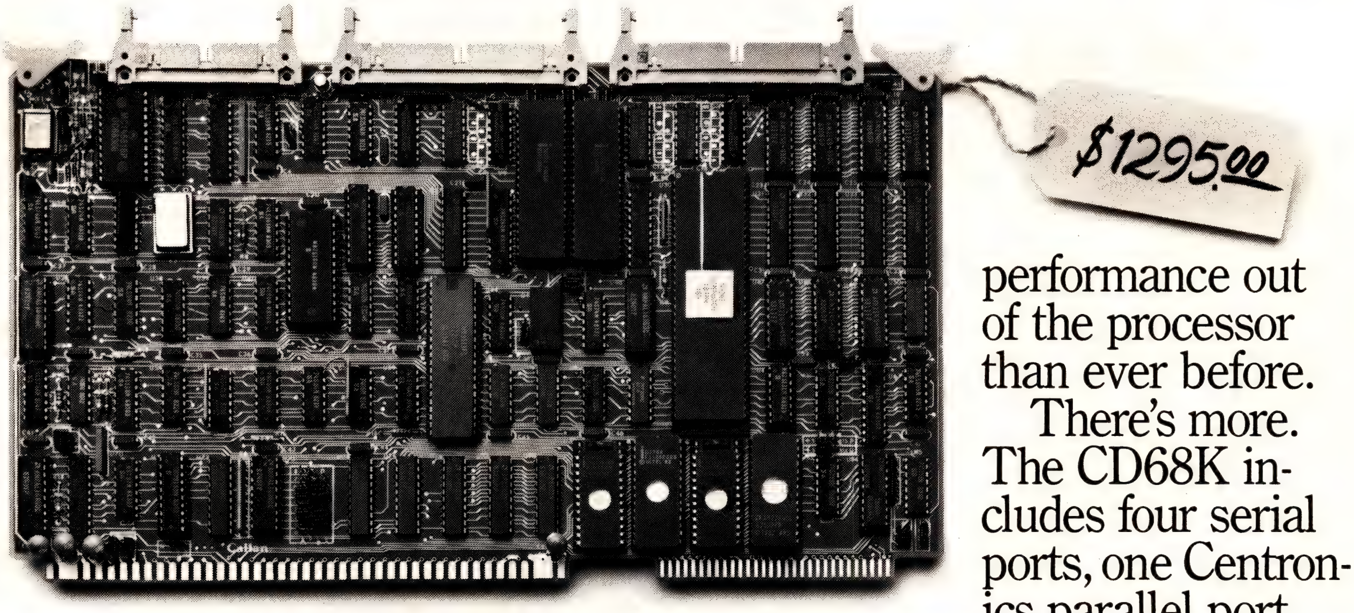

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- **Performance Budgeting** options—available only with TI's Advanced Schottky Family of ALS/AS devices—optimize your system speed/power product (*Page* 3).
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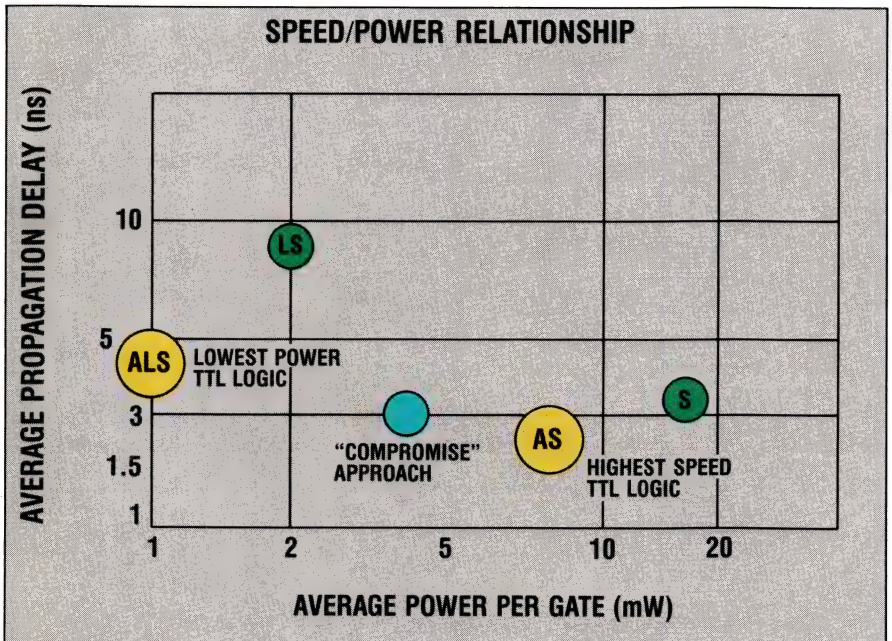

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AS functions: World's highest speed TTL

When speed is your top TTL priority, TI's AS logic is your best choice. With a typical 1.7-ns gate delay and only 8-mW power dissipation per gate, AS logic is faster than a compromise approach to TTL (see above and at right). And TI offers you a wide choice of AS logic devices.

In addition to the high-speed 'AS881 and 'AS882 devices used by Data General, there are also the following new, very fast, 8-bit, byte-oriented ICs:

'AS870/'AS871 register files contain internally multiplexed, dual, 16-word by 4-bit data sources for direct ALU input. Plus, multiplexed I/O ports minimize processor data-path access times to memory and system bus structures.

The 'AS877 octal transceiver provides both parallel and serial ports for system interconnection. Its integral serial data port simplifies fault detection and reduces system debugging.

'AS867/'AS869 octal bidirectional counters are fully paralleled, high-performance, presettable 8-bit counters that minimize next-address generation compromises. Both asynchronous and synchronous clear versions are offered.

Many more AS logic devices available from your TI distributor are listed on the next page.

ALS functions: Lowest power TTL

Is low power your key TTL requirement? Then TI's ALS devices are your best solution. They give you absolutely the lowest power—1.2-mW gate power dissipation—plus very respectable speed at 4-ns gate delay, typically. ALS logic typically requires 68% less power than a compromise-logic approach, with only 25% less speed.

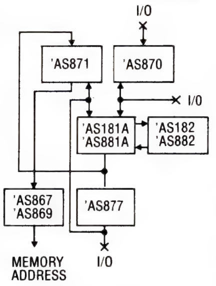
TI packaging options include unique 68-pin plastic chip carrier

Need higher complexity functions for your new designs? Or pin-for-pin equivalent functions for easy system upgrades? TI's broad Advanced Schottky Family of ALS/AS devices gives you both.

Most members of the Advanced Schottky Family are available in 14-pin, 16-pin, 20-pin, and the new 300-mil-wide, 24-pin DIPs. Also, the family now comes in surface-mount 20-pin, 28-pin, 44-pin, and TI's unique 68-pin plastic-leaded chip carriers.

Arithmetic Processor

TYPICAL DATA PATH
Throughput Time (ns)



Word Length	8 bit	16 bit	32 bit
Register File	12	12	12
ALU	10	14	19
Accumulator/ Address Generator	10	10	10
Total Through-put Time	32	36	41

Higher throughput at the component level and more architectural features enable you to increase overall system performance with TI's high-speed AS logic.

Use of the new surface-mount chip-carrier packages can almost double functional densities. Board space can also be reduced by using the new 300-mil-wide, 24-pin DIP versus the industry-standard 600-mil-wide package.

For more information on TI's Advanced Schottky Family of ALS/AS logic, return the coupon on the next page.

See back page for more information.

ronment, at least in the forseeable future, as host-machine based—but he sees it networked to smaller work stations that have substantial stand-alone capability. "From a strictly practical point of view, it doesn't really matter who makes the host computer," he adds.

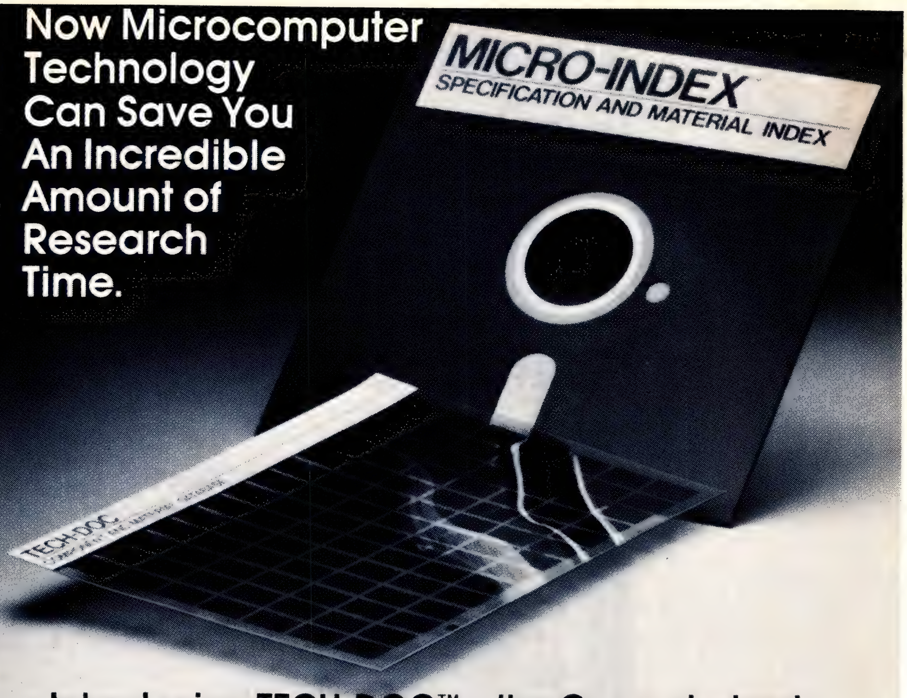
Three areas. Taku says DEC will concentrate on applications, operating systems, and networking to achieve its goal of providing the end user with a horizontally integrated CAD/CAE environment. Efforts in each area would seek to reconcile the design engineer's need for his own work station—each with a powerful central processing unit, to which he could have ready access—with the need to keep the cost of the work stations down—as well as to avoid incompatibilities between work station and host computer.

The high speed of transmission (70 megabits per second) across the DECnet-Ethernet system should enable any designer using the system to perform schematic entry at the work-station level, transfer it to the host computer for simulation and logic testing, and get it back in plenty of time to make the necessary changes.

This interchange, according to Taku, provides each design team member with a "window to the whole engineering network." It is a real-world alternative to the more expensive approach of doing logic simulation on large (and costly) individual work stations.

That window will be enlarged by two additional developments that DEC is planning to announce at Albuquerque: the VT 241 terminal, which permits the review (and some editing) of any design on the system from anywhere else in the system; and greater compatibility between DEC's Rainbow 100 Plus and Pro 350 personal computers with the VAX operating system.

The personal-computer link is DEC's way of recognizing that much of an engineer's work consists of administrative tasks as well as of actual design. By cross-referencing those two areas and by extending DECnet and VAX operating-system architecture down to the level of the work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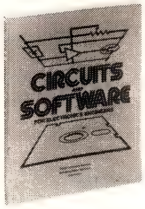

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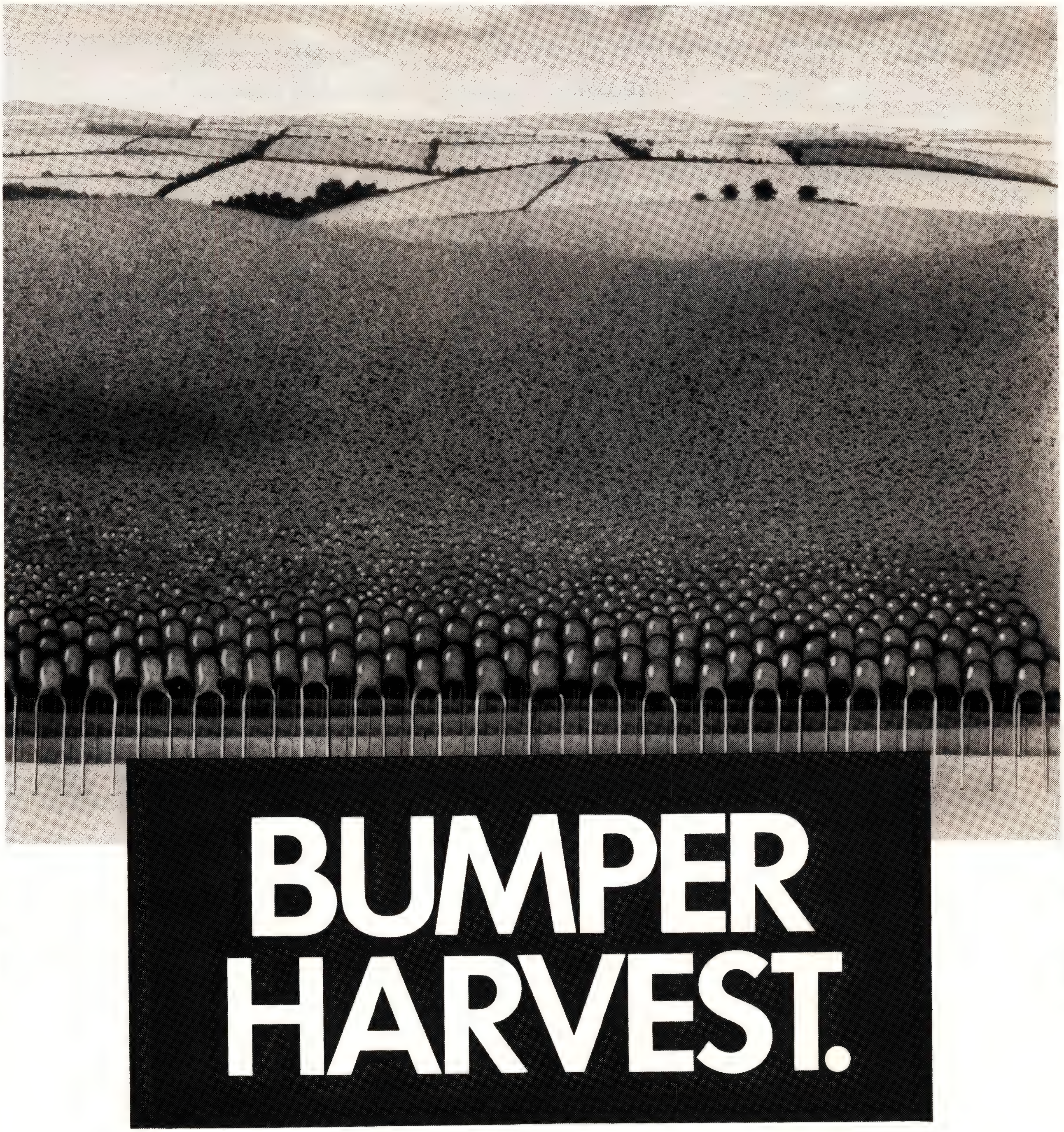

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SCIENCE/SCOPE

NASA's Project Galileo Probe, which will explore the planet Jupiter later this decade, must arrive at a precise angle if it is to carry out its measurements of the chemical composition and physical state of the Jovian atmosphere. The Hughes Aircraft Company-built probe will arrive at 107,000 miles per hour, fast enough to travel between Los Angeles and Las Vegas in nine seconds. If the probe hits at too shallow an angle, it will skip off into space; too steep, it will be reduced to ashes. Even at the proper angle, the probe will encounter extremes never before faced by spacecraft. In less than two minutes, much of the forward heat shield will be eroded by temperatures of thousands of degrees. With atmospheric entry forces reaching 360 times the gravitational pull of Earth, the 742-pound probe will take on a weight equal to an empty DC-10 jetliner. Project Galileo is set for launch from the space shuttle in May 1986 and to arrive in August 1988.

The improved Phoenix missile virtually thinks for itself, thanks to advanced digital electronics. The radar-guided missile, carried by the U.S. Navy's F-14 Tomcat fighter, is the primary long-range air-to-air weapon for fleet defense. The new AIM-54C model contains 55 types of hybrid circuits—a combination of integrated circuit chips with discrete devices. They pack five or six times more computer instructions into the missile and allow it to process information hundreds of times faster. In addition, digital processing will accommodate modifications easily. As new missions are defined to meet new threats, new program memory cards can be plugged wihout rebuilding hardware. The missile is in low-rate production at Hughes.

Computers are helping to design and build satellites, thereby saving time, effort, and costs. One use of computer-aided design/computer-aided manufacturing at Hughes has been in developing a technique to bend titanium tubes used in propulsion systems. Design information in one computer was transferred to another and turned into three-dimensional graphics to verify that there were no physical interferences in the routing. The technique has substantially cut design and drafting efforts. Future plans include adding a computer-controlled tube bender that will directly accept computer instructions.

A laser that won't cause blindness or other eye injuries will be used in a rangefinder now under development by Hughes for the U.S. Army. The lightweight device, designated the AN/PVS-6 Mini Eyesafe Laser Infrared Observation Set (MELIOS), resembles a binocular case. Its neodymium yttrium aluminum garnet laser beam is sent through a chamber, or cell, filled with high-pressure methane gas. There the 1.06-micron frequency is transformed into a frequency of 1.54 microns. The new signal is safe because it never reaches the retina, but instead is absorbed in the vitreous humor, the white area of the eye between the retina and the lens. MELIOS is being developed under a competitive contract from the U.S. Army Night Vision and Electro-Optics Laboratory.

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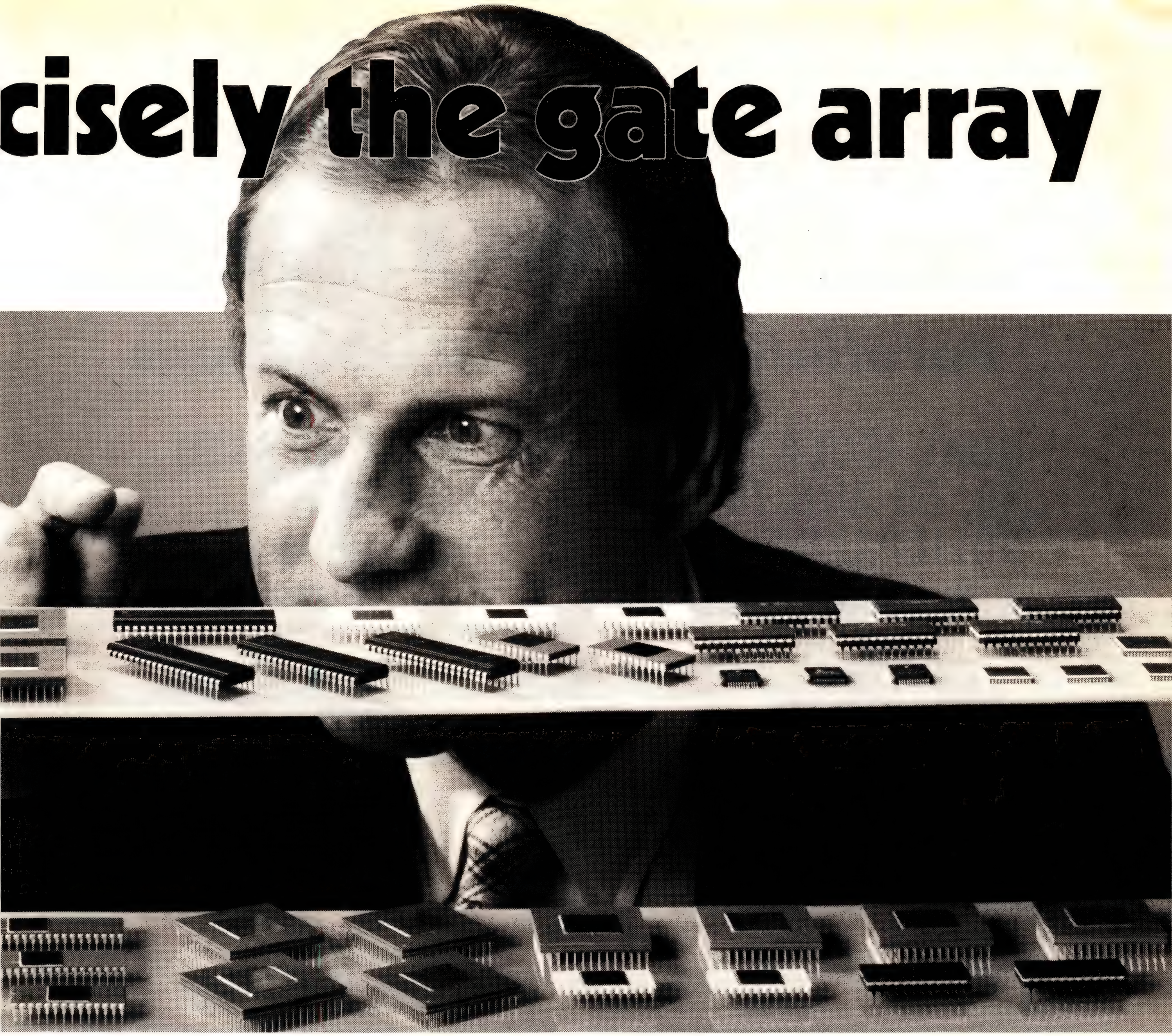

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Fujitsu Gate Arrays

Technology	Device	Complexity	Signal Pin (Max)	Delay Time (Typ.) (Internal Cell)	Power Dissipation
Si-Gate CMOS Gate Array	C-440H	440(2-input)	54	4.0ns	50mW/PKG at 10MHz
	C-770H	770(2-input)	70	4.0ns	50mW/PKG at 10MHz
	C-1275H	1275(2-input)	80	4.0ns	50mW/PKG at 10MHz
	C-2000H	2000(2-input)	68	4.0ns	50mW/PKG at 10MHz
	C-2600VH	2640(2-input)	106	2.5ns	50mW/PKG at 10MHz
	C-3900H	3900(2-input)	68	4.0ns	100mW/PKG at 10MHz
	C-3900VH	3900(2-input)	127	2.5ns	100mW/PKG at 10MHz
	C-8000VH	8000(2-input)	160	2.5ns	100mW/PKG at 10MHz
LSTTL Gate Array	B-240	240(3-input)	40	1.9ns	0.8 mW/cell
	B-350	360(3-input)	48	1.9ns	0.8 mW/cell
	B-600	616(3-input)	64	1.9ns	0.8 mW/cell
	B-1100	1120(3-input)	88	1.9ns	0.8 mW/cell
	B-2000	2108(3-input)	112	1.0ns	0.65mW/cell

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Adapso launches war on software piracy

Adapso, the Association of Data Processing Organizations, is putting together a war chest for a broad-based offensive on software piracy. With an operating fund that already totals $200,000, **the association wants its 700 members to support the effort with contributions of up to $50,000 per company.** Some of that money will be used to produce educational materials, such as a video tape, that will be made available at next month's National Computer Conference for use by member companies and their customers. "It's time for a user's bill of rights on the issue," says Steve Ballmer, marketing vice president of Microsoft Inc., Bellevue, Wash., and co-chairman of the fund. In addition to supporting publicity and educational activities, the new kitty, called the Software Protection Fund, will be used to aid members in the area of enforcement by establishing an expert-witness program and filing friend-of-the-court briefs in appropriate cases.

U. S. to spend billions on information systems...

The U. S. Government will spend more than $29.8 billion over the next six years to purchase, operate, and maintain some 1,500 new computer and telecommunications systems costing over $1 million each, says the Office of Management & Budget. Of the total, about half will go to commercial suppliers for services that include systems analysis, design, and programming. **The Department of Defense continues to be the biggest buyer, accounting for 30% of total expenditures;** the General Services Administration comes in second, at 25.6%; and the National Aeronautics & Space Administration is third, at 10.8% (see p. 115).

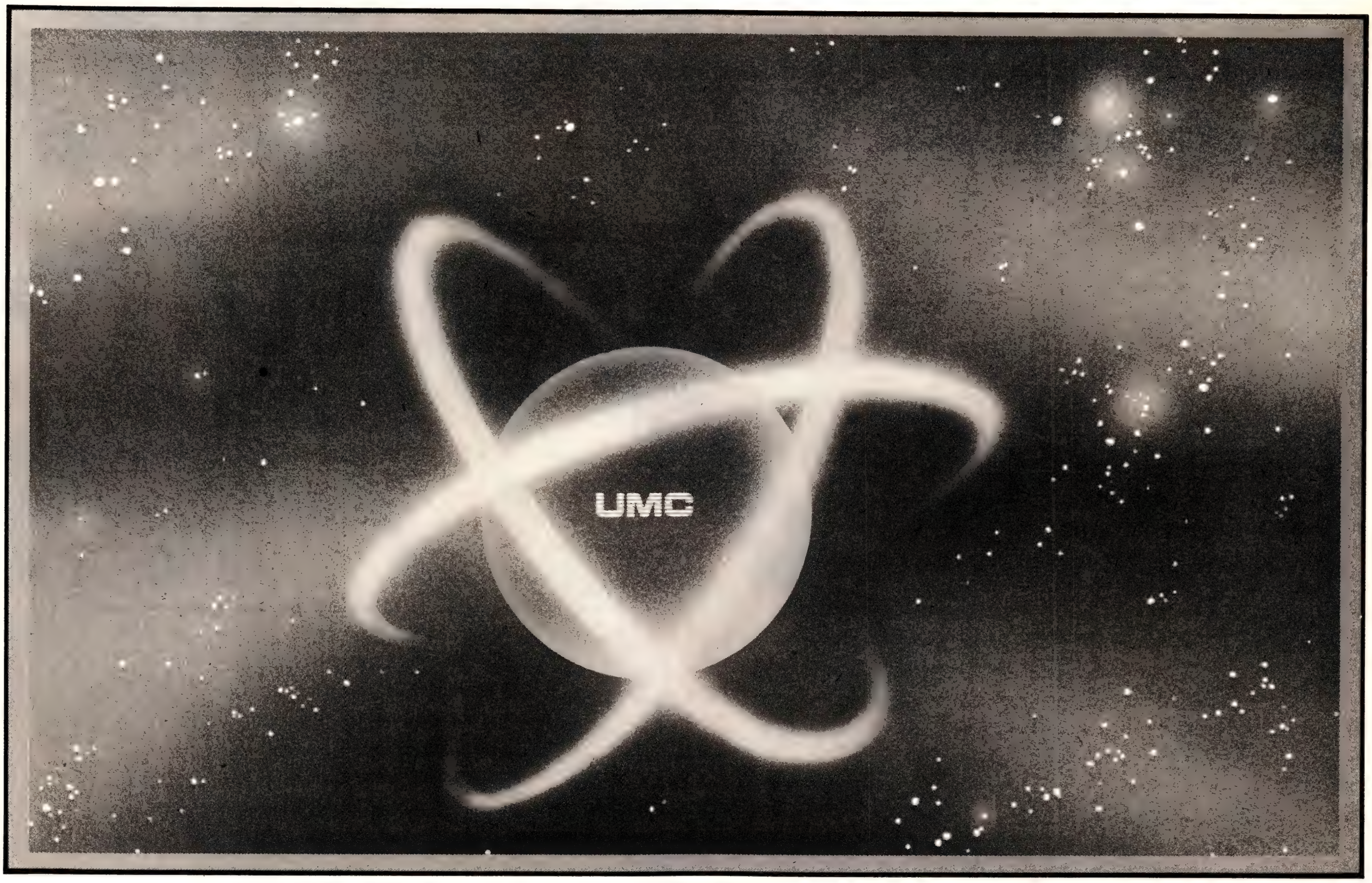
...as OMB worries about rhyme and reason

With individual agencies laying out hundreds of millions of dollars each for new data-processing systems, the Office of Management & Budget is increasingly concerned that "technologies be acquired and used in a rational way," according to an OMB report. **In many cases, frets the agency, planning is driven by the availability of money rather than the "real-world environment of the agency."** As a consequence, systems are "developed incrementally without regard for longer-term considerations, or they are patched and fixed to meet short-term needs."

Industry, Government differ on size of software market

Sounding an optimistic note, the Association of Data Processing Servicing Organizations predicts that the Federal government will buy $41 billion worth of software and related services by 1990, nearly double what the Government itself expects to spend (see p. 108). **Somewhat closer to Uncle Sam's expectations is the trade group's forecast of a $10.3 billion market by 1985,** $2.2 billion less than estimates from the Office of Management & Budget. In all markets, annual revenues of the U. S. computer-services and software industry grew by 21.4% from 1982 to 1983, rising from $27.6 billion to $33.5 billion, and will reach $90 billion by 1988, says Adapso. By industry segment, it reports revenues from software products grew 39% from 1982 to 1983, as well as 18% in turnkey systems, 20% in professional services, and 13% in data-processing services.

UMC-The nucleus of MOS ICs



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International newsletter

France looks to lessen dependence on U. S.-made telecom components . . .

CIT-Alcatel, the telecommunications switch manufacturer controlled by the French government, is moving to lessen its dependence on foreign-manufactured components—a step that could give the edge to SGS-Ates Componenti Elettronici SpA, the Agrate, Italy, company competing with Harris Semiconductor Corp. to supply chips for the Parisian firm's subscriber-line interface card. **Both foreign firms have development contracts with CIT-Alcatel for their respective SLICs,** but the Italian company is planning to produce its version at a factory at Rennes, in Brittany, while Harris production is now limited to Melbourne, Fla. The U. S. company's French joint venture with Matra SA, Matra-Harris Semiconducteurs, in Nantes, uses only Harris's MOS technologies, not the dielectric-isolation process in which its SLIC circuit has been designed. For SLIC microprocessors, CIT-Alcatel is expected to turn from the Intel-supplied parts it is currently using to Thomson Semiconducteurs, which will produce one of the Motorola families at a plant located in Grenoble.

. . . while Zenith expands its role there

The Compagnie de Signaux et d'Entreprises Electriques has signed an agreement with Zenith Radio Corp. whereby the Parisian company will assemble Zenith's Z100 personal computer, an 8088-based machine said to be highly compatible with the IBM Corp. Personal Computer. **The CSEE-produced computers will be used in the company's own systems, principally military and transportation,** and will also be sold by Zenith's French subsidiary, Zenith (France) SA. Assembly of the computer is expected to begin next year at the company's plant in Périgeux, where CSEE already carries out assembly operations for IBM.

Siemens plans 256-K RAM

Siemens AG, joining the small band of semiconductor producers offering a 256-K dynamic random-access memory, already has a 1-Mb RAM in the initial design stage. **The Munich-based firm is now gearing up its facilities in Villach, Austria, for volume production of the part next year and will thus become the first European company to offer a 256-K chip.** The HYB41256 has a 1-bit organization, operates off a single 5-V supply, and is made with the company's high-performance n-channel silicon-gate technology. A proprietary chip cover guards against alpha radiation. The RAM will come with access times of 120, 150, and 200 ns. Nine multiplexed address inputs make it possible to place the 41256 in an industry-standard 16-pin dual in-line package.

Printer duplicates 2-hour video tape in 90 seconds

Sony Corp. is introducing a high-speed video-tape printing system called Sprinter, which can copy a 2-hour Beta-format program in 90 s. **The Tokyo firm also developed a new metal tape with a high coercivity of 2,000 oersteds for the system,** which features an air-bearing drum with a hollow-core head that blows a small stream of air at the tape in order to hold tape position to micrometer tolerances. As the master and blank tapes pass around the drum one on top of the other, a magnetic field is applied, instantly duplicating the video and audio signals. Because the hollow-core head does not touch the tape, the head's life is lengthened—from a typical 500 hours to "semipermanent," the company says.

For reliable surface-mount packaging, rely on TI's copper clad Invar.

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What's more, TI's copper clad Invar foil is far more cost effective than other low-expansion alternatives.

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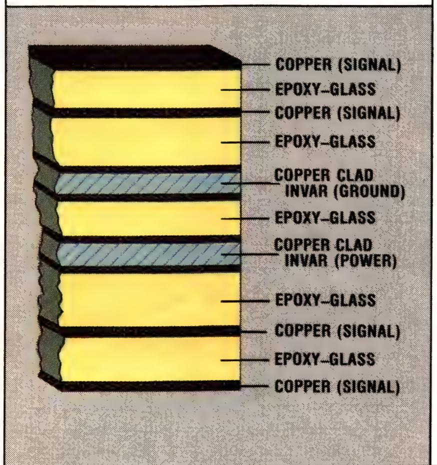

Others have already gained the advantages of surface-mount technology and are in full production today! So why wait? Put TI's copper clad Invar foil to work for you today.

For more information and a list of sources for treating and lamination, write Texas Instruments Incorporated, Dept. MMN873EC, P.O. Box 402250, Dallas, TX 75240. Or call 1-800-341-5202.

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Electronics international

Significant developments in technology and business

Digital techniques in correction circuits sharpen TV picture

by John Gosch, Frankfurt bureau manager

Added to digital chip set, new circuitry eliminates hoizontal distortion and cuts component count

By applying digital techniques to the correction circuitry for a TV screen's east-west distortion, horizontal-linearity distortion, and convergence distortion, designers at West Germany's Intermetall GmbH, lead house of the ITT Semiconductors group, have significantly raised the picture-sharpness and beam-focusing performance of digital TV receivers.

Thus the Freiburg-based group, the pioneer of digital TV, has struck back at its critics and competing chip makers. These parties have long maintained—perhaps rightly so—that in its present form ITT's digital approach to receiver design results in no discernible improvement in picture quality, although it does make for reduced components count, fewer factory adjustments, and thus for more streamlined set production [*Electronics*, April 5, p. 89].

In conventional analog receivers, east-west distortion, evidenced by the field's left and right edges bulging inward, is corrected by modulating the horizontal deflection current. A similar remedy is applied to horizontal linearity distortion, which shows up in unequal spacing between vertical lines. Convergence distortion, on the other hand, which manifests itself by the red, green, and blue electron guns producing mismatched fields, is corrected by adjusting the magnetic lenses for the three electron beams.

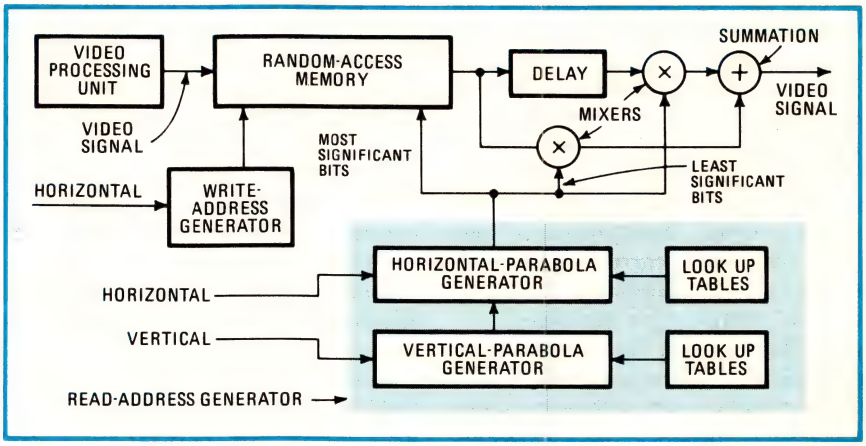
Despite these correction methods, however, errors remain, and the various types of distortion are still visible, especially in the corners of the screen. With digital techniques, correction functions can easily be implemented and nonlinear errors eliminated, maintains Rolf Deubert, head of project engineering at Intermetall. The result is a much-improved picture quality, with all details well-defined across the entire screen.

Simplification. Besides providing better picture quality, the ITT approach reduces the components count in the correction circuitry, as it obviates the need for the east-west modulator and the linearity coil. Further, in tube production, it simplifies—or possibly eliminates—the need to match the deflection system to the tube because all residual errors are automatically corrected by the digital correction circuitry in the set.

The new concept, which Deubert discussed at the June 6 to 8 International Conference on Consumer Electronics in Chicago, is being implemented in ITT's second-generation Digit 2000 chip set. This two-chip set is expected to be in silicon at the end of the year.

In the new ITT implementation, correction is limited to horizontal distortions. To handle the less serious vertical distortions as well would require a somewhat expensive line store, so these errors are still adjusted by conventional means.

East-west distortion produces a field consisting of horizontal lines of different lengths. By modulating the timing of the video signal, the ITT concept produces a rectangular picture within the field, with all its lines being of equal length. Thereby the distortion is corrected. Horizontal-linearity distortion is corrected as well for either the red, green, or blue signals. Since each signal must be corrected separately, three such circuit blocks are needed, and together



Triplicate correction. ITT's new digital circuitry corrects east-west as well as horizontal-linearity distortion for either the red, green, or blue signals. Since each signal must be corrected separately, three such circuit blocks are needed, and together they perform the convergence correction for the RGB electron beams.

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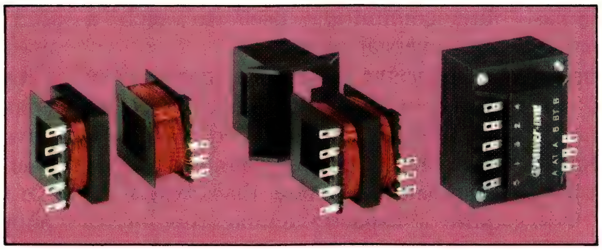

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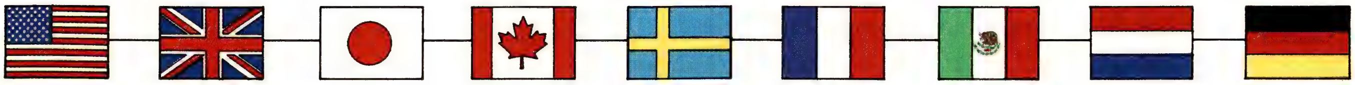

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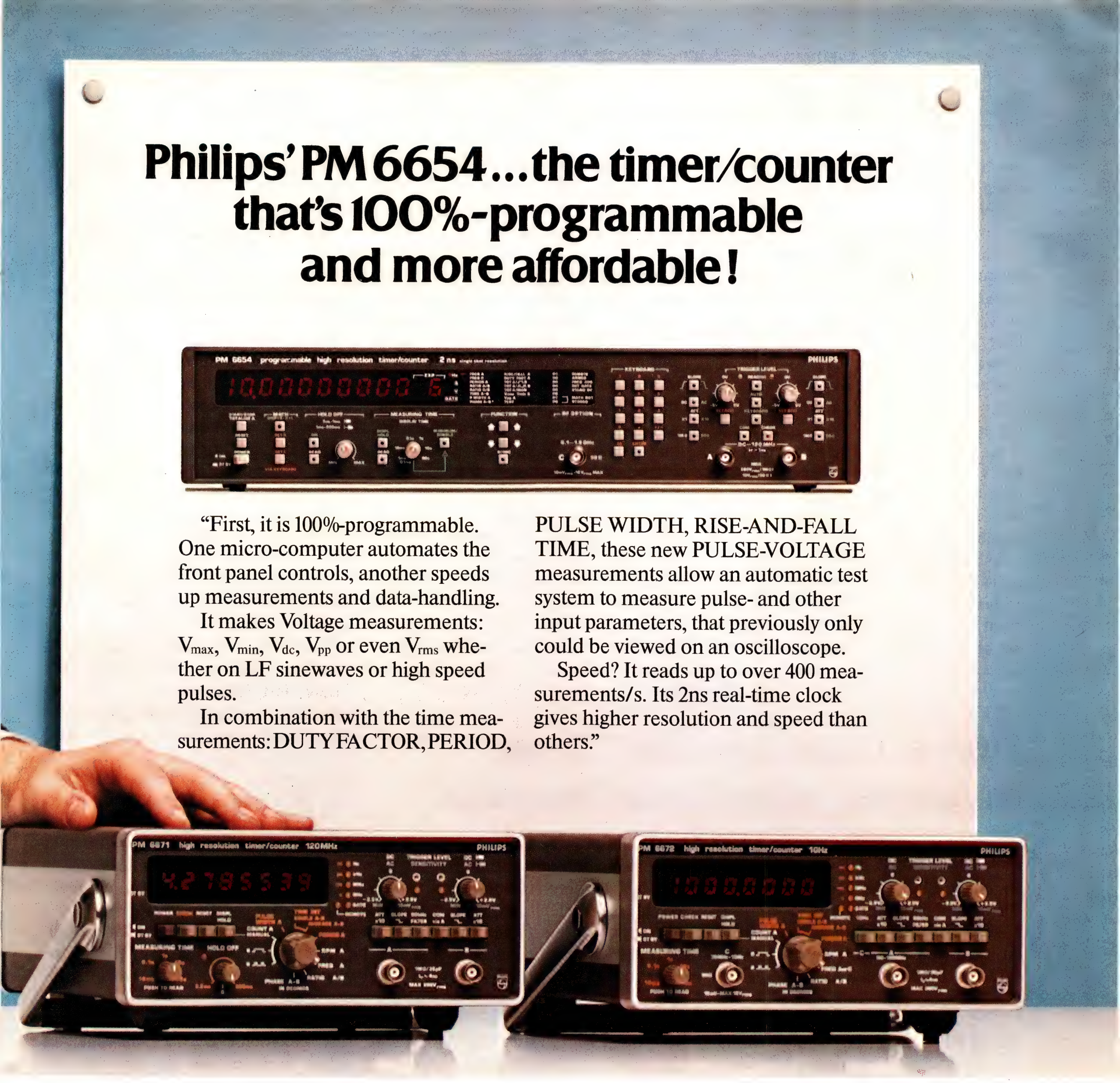
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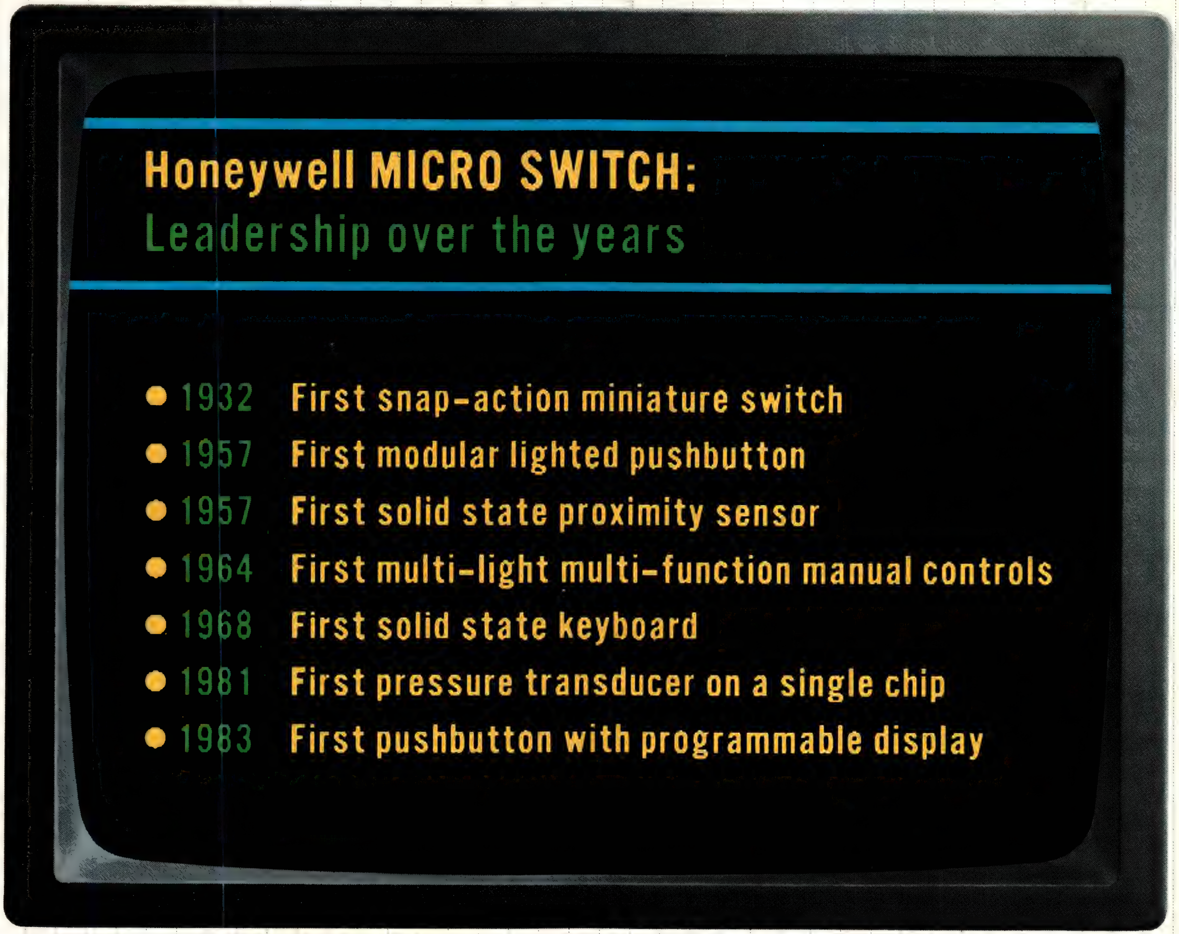

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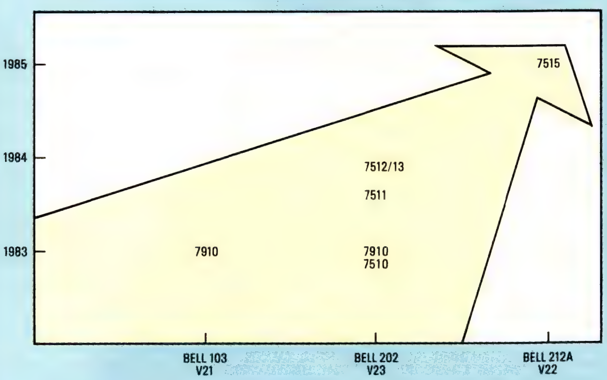

EFB 7512/7513
FSK modem: V23 - CMOS technology - transmission speeds: 75, 1200 Bauds - reception speed: 75, 1200 Bauds - power supply: ± 5 V. Includes modulation, demodulation, filter functions, interfaces (V24/RS232, V25 and V54) - Designed for turnaround applications - 22-pin plastic case.

EF 7910
FSK modem: BELL 103/113/108/202 and V21, V23 - HMOS technology - Programmable for speeds of 300, 600 and 1200 Bauds - power supply: ± 5 V. Includes modulation, demodulation, filter functions, the main RS 232/V24 handshake signals and automatic answering capabilities - Videotext and teletype compatible - second source of AMD - 28-pin Cerdip case.

EFG 7515
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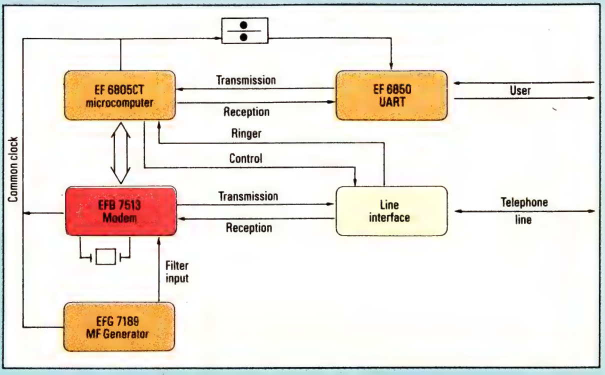

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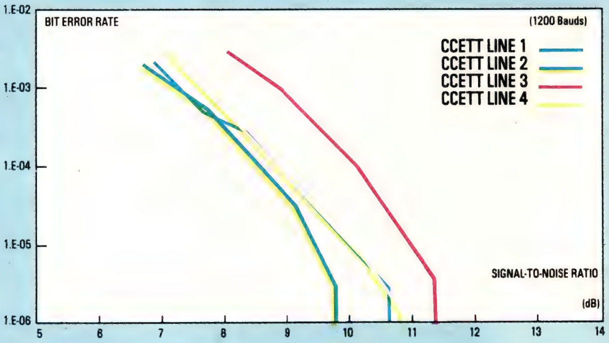

COMMUNICATION PERFORMANCE: EFB 7512

Typical error rate measured at 1200 Bauds for EFB 7512 on lines representative of the French network (CCETT 1, 2, 3, 4) in compliance with CCITT Recommendation V 52. Tests conducted in Thomson Semiconductors laboratory in Grenoble. Identical measurements are conducted for lines representing the Italian network (SIP 1, 2, 3, 4), the British network (BS 6305), the German network (FTZ) and the American network (FCC lines 3002 C1, C2, C3, C4 conditioning).

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Magarshack goes public with Thomson GaAs ICs

John Magarshack is nearly ready to go public. Appointed in 1980 to establish a department at the Thomson-CSF Microwave Components division to commercialize gallium arsenide integrated circuits, he is about to take the company into the production phase of his five-year plan, at a time when GaAs ICs are still very much a laboratory animal.

Being able to envisage production so soon is a direct result of Thomson's starting GaAs IC research as early as 1974 at its Central Research Laboratory in the Paris suburb of Corbeville, from where Magarshack, 52, directs the development operation as manager of Gallium Arsenide Integrated Circuits. By 1980, the research team had reeled off a string of successes encouraging enough to justify wooing Magarshack away from GaAs research at the Laboratoires d'Electronique et de Physique Appliquée, Philips' principal French research laboratory, to begin funneling Thomson's research toward more profitable ends.

Magarshack's plan consists of three phases. The first and most demanding was devoted to small-scale production aimed at exploring the parameters of the company's enhancement-mode planar process, developing computer-aided-design tools, and establishing automatic-measurement routines.

That work was completed early this year, opening the way for the current preproduction phase, in which the process steps will be defined rigorously "from A to Z." More importantly, though, Magarshack's department will begin its first real contact with customers.

"We've got about 14 different projects with customers going at the moment, most of them internal" (in different Thomson divisions), reports Magarshack. "We find that our internal needs break down into a 50-50 split between logic and microwave. An Englishman, Magarshack studied physics at Cambridge University and worked in his native country in both the textile and nonferrous-metals industries before being hired by Philips in 1963 to go to France. He first began working in semiconductor research in 1966, and with GaAs ICs at LEP in 1977 before moving on to Thomson.

Breaking out. John Magarshack is nearly ready to commercialize gallium arsenide integrated-circuit production at Thomson-CSF.

Kretzschmar's courage tempered by acumen

An eye-catching item in Ulrich Kretzschmar's office is the coat of arms of his wife's family, whose origins go back to a 14th-century Austrian landowner. One of the emblems in the heraldic picture is a lion, the symbol for courage.

Courage is what the 30-year-old Kretzschmar had when he left a secure sales position at a German computer firm to strike out on his own. "I couldn't do what I wanted to do, as I was subject to company policy or majority decisions," he says. So on April 1 of this year, with no outside financial backing, he set up ASCI Computer GmbH in his one-family house in Ottobrunn, a Munich suburb, "to realize my own ideas."

Unusual. Ulrich Kretzschmar, leaving a secure job to go it alone, took an unusual route for a young German engineer.

Kretzschmar's company is active in the market for products compatible with systems from Digital Equipment Corp., the U. S. computer maker. His four-person firm analyzes a customer's technical or scientific data-processing problems and sells the equipment to solve them. The customers are industrial firms, universities, and research institutes in West Germany, Austria, and Switzerland.

ASCI's products comprise about 80 items, from plug-in modules and peripherals to terminals and software packages, with the emphasis on data-acquisition and graphics applications. The equipment comes from outside suppliers; installation and service are handled by an outsider as well, "because we are still too small to get into that rather cost-intensive side of the business," Kretschmar says.

With this strategy, Kretzschmar, a graduate of Frankfurt's Control Data Institute, who put in a two-year stint at DEC in Munich, hopes to gross some $300,000 by the end of this year and $800,000 in 1985. "Our near-term goal is to grow until we are 15 people and then consolidate our business before we move on."

By consolidation, he means acquiring enough cash reserves to enable the firm to ride out any downturn in sales. "We don't want to push growth at all costs," he says.

To many people, that may sound too cautious a policy for an electronics firm. But he points to some companies in the fast-paced computer business that no longer exist because they misread the market and overextended themselves without sufficient funds to finance growth.

To avoid that, "we want to put our firm on a solid footing before we take the next step," Kretzschmar says. Such a philosophy would be in line with the meaning of another emblem in his wife's coat of arms—a fish, the symbol for prosperity.

...the Facts

Not claims but hard facts. Facts about SGS Power – manufacturing capability and range of products, worldwide sales and service organisation and, of course, about technology. For example, the SGS combination of Full Mesa and Multiepitaxial technologies gives rugged and reliable High Voltage transistors.

Facts about SGS Power

1 Wide range of over 1000 standard types, covering almost every application, and growing by not less than 1 new type every day.

2 Many innovative new products, including High Voltage up to 1500V, Power MOS types and high power modules up to 35kVA.

3 Seven volume packages – TO-126, SOT-82, TO-220, SOT-93, TO-39, TO-3 and TO-240.

4 5″ wafer capability, ion implantation and other state-of-the-art technologies.

5 Three manufacturing locations in Europe and two in Asia.

6 Availability and service from Sales Offices and Distributors worldwide.

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Tel: 039-65551 Tlx: 330131-330141

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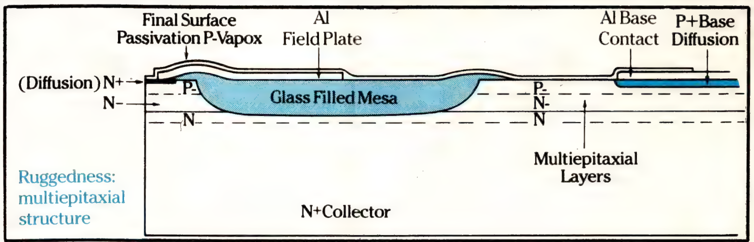
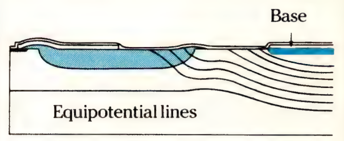
Facts about rugged and reliable High Voltage transistors – from SGS

Multiepitaxial technology is unique to SGS, while few other companies can claim the advantages of Full Mesa. But SGS offers the two technologies combined, to achieve exceptional ruggedness and reliability.

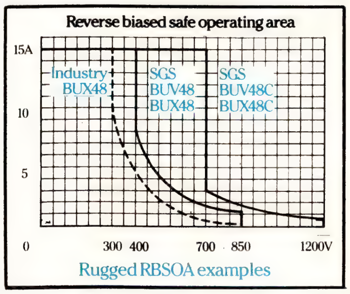


Ruggedness: multiepitaxial structure

Thanks to Full Mesa Channel technology, the wafer can be cut outside the Mesa. So glass crack hazards are eliminated.



Reliability:low stress electric field



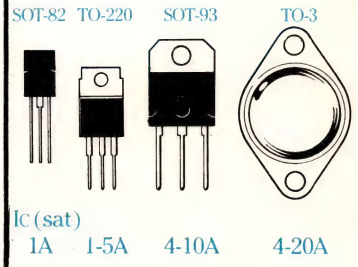
Rugged RBSOA examples

Multiepitaxial technology gives very close control of voltage ratings and optimizes ruggedness when switching inductive loads.

V_{CEO}	400 – 700V
V_{CES}	700 – 1400V

(1500V being sampled)

High voltage transistor packages



Technology and Service

Like every SGS Power device, all High Voltage transistors are available from our worldwide sales organisation. So why not prove these facts for yourself? And gain from our world leadership in Power technology.

Circle 228 on reader service card

Controller for Winchester disk drive has data buffers on chip

by Michael Berger, McGraw-Hill World News

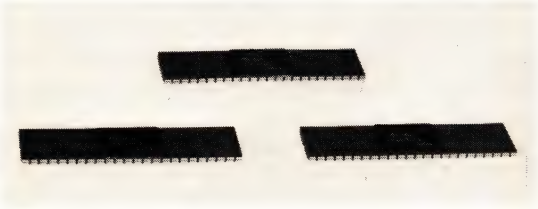
C-MOS chip uses a set of 21 high-level commands for disk control and dot transfer, also does error detection

Versatility is the word for Hitachi Ltd.'s newly developed hard-disk controller, which incorporates data buffers on chip. The HD63463 also includes advances in the data-transfer rate, buffering, and error correction, along with a set of 21 high-level commands for data transfers, drive control, buffer management, diagnostics, and the like.

The controller, a peripheral member of Hitachi's 16- and 32-bit HD68000 microprocessor family, also can interface to drives based on both ST506 and Storage Module Drive standards. It can handle up to four 5¼-in. and eight 8-in. Winchester disk drives, but not in combination, and also handles parallel seek, multisector, and multitrack operations. The drive format is programmable, including up to 1,024 cylinders per drive and sector lengths from 256 bytes to 4-K bytes.

The 7.02-by-8.94-mm integrated circuit, fabricated with 2-μm complementary-MOS geometries, reaches a maximum data-transfer rate of 20 megabytes/s using nonreturn-to-zero encoding or 10 megabytes/s using modified frequency-modulated encoding. It owes its speed to the arrangement of two 256-byte data buffers, which the host microprocessor and the disk can access simultaneously or separately. Since the data buffers decouple the host processor from the data-transfer process, a wider range of system functions is available.

Major data-buffer functions include two fully programmable codes for error detection and correction. The 16-bit cyclic-redundancy-checking code provides for error detection only, making it possible to make corrections in programming, and the 32-bit error-correction circuit can detect and correct burst errors up to 11 bits long. Because of the buffer, error correction can be performed in parallel with other system activities, thereby requiring no microprocessor overhead.



The HD63463—available in 4-, 6-, and 8-MHz models—operates from a single 5-V supply, requires 250 mW for typical operations, and is fully TTL-compatible. It is housed in a Joint Electron Devices Engineering Council standard 48-pin dual in-line package. The controller also has both a 16-bit data bus, for interfacing with the Hitachi 68000 processor, and an 8-bit bus mode, for compatibility with parts having lower performance.

The HD63463 is priced at $44, $74, and $87 for the 4-, 6-, and 8-MHz versions, respectively. Samples will be available this autumn. For large quantities, scheduled to be available next January, delivery will take four to eight weeks from receipt of order.

Hitachi Ltd., Semiconductor & Integrated Circuit Division, New Marunouchi Bldg., 5-1 Marunouchi 1-Chome, Chiyoda-Ku, Tokyo 100, Japan [Circle reader service number 442]

Six-layer card holds computer, has room for 16-K bytes of RAM, plus PROM

As electronics gets ever more pervasive, real-time microcomputer controllers are turning up in more and more systems—and more often than not, there is a requirement for a low-power microcomputer controller taking up a minimum of space. That is where the LM 101 comes in.

By using a six-layer printed-circuit board, Burndept Cyfas Systems Ltd. has packed a complete single-board microcomputer on a card measuring 6.44 by 2.24 by 0.52 in. The LM 101 comprises a complementary-MOS 8085 central processing unit clocked at 6 MHz, with room for up to 32-K bytes of plug-in erasable programmable read-only memory to store the microcomputer-control program, and capacity for up to 16-K bytes of random-access memory.

Targeted at real-time control applications, the board has dual timers and a software interrupt facility. For communication over a serial link, there is a universal asynchronous receiver-transmitter chip.

All the bus lines, address, data,

SIEMENS

The MKV commutation capacitors:

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Your thyristors should turn off. So they need reactive power. Their short turn-off times (15 μs) lead to short circuit-commutating times (28 μs).

MKV commutating capacitors from Siemens provide the reactive power necessary in these minute fractions of a second.

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- very low-ohmic loss of approx. 1 mΩ
- unequalled current-carrying capability – typically 300 V/μs

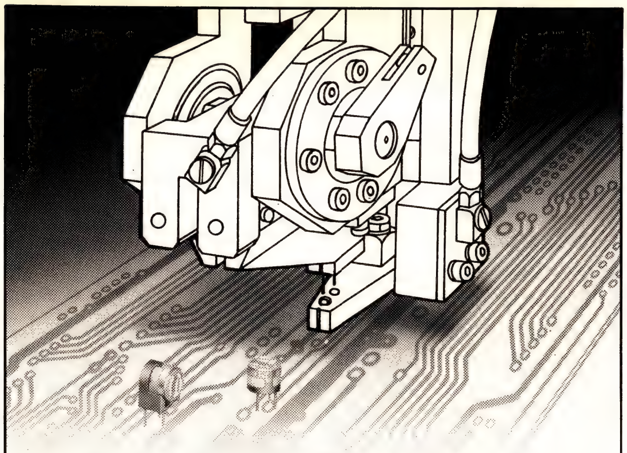
The fuse in all MKV capacitors prevents shorting and thus destruction of commutating thyristors.

If you want to find out more about Siemens capacitors for power electronics, write to Siemens AG, Infoservice/B 8411, Postfach 156, D-8510 Fürth, West Germany, quoting "Capacitors for power electronics".

Siemens – a world power in capacitors

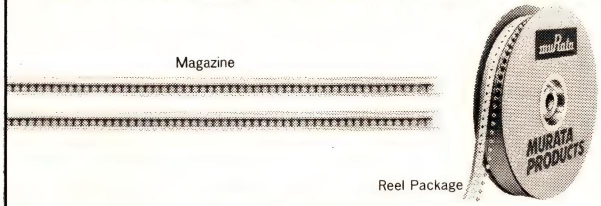
B8411.101

Circle 230 on reader service card



ADJUSTMENT POTENTIOMETER

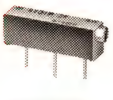
MURATA'S CERASTAT®
FOR AUTOMATIC INSERTION



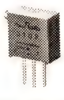
ADJUSTMENT POTENTIOMETER

CERASTAT®

Murata's CERASTAT® trimmer potentiometers offer both high precision adjustability and outstanding temperature characteristics. And that's why CERASTAT® is today used in a wide range of computer and communication equipment, and for fine adjustment of circuits in and other devices.
CERASTAT® potentiometers meet the needs of advanced electronics from consumer to industrial use, offering a large selection of terminal configurations and a high degree of design freedom. CERASTAT®'s structure brings to life new ideas, while its waterproof construction enables ultrasonic cleaning.
Moreover, these potentiometers are ultra-small and very low priced. Taped CERASTAT®'s are available for use with various automatic inserters.


POT2101P

POT3102Y


POT3102X

3321H

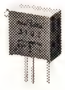
3321P

3321N

POT1102P

POT1102S

3102W


3102Z

POT3104H

POT3104P

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Circle 231 on reader service card

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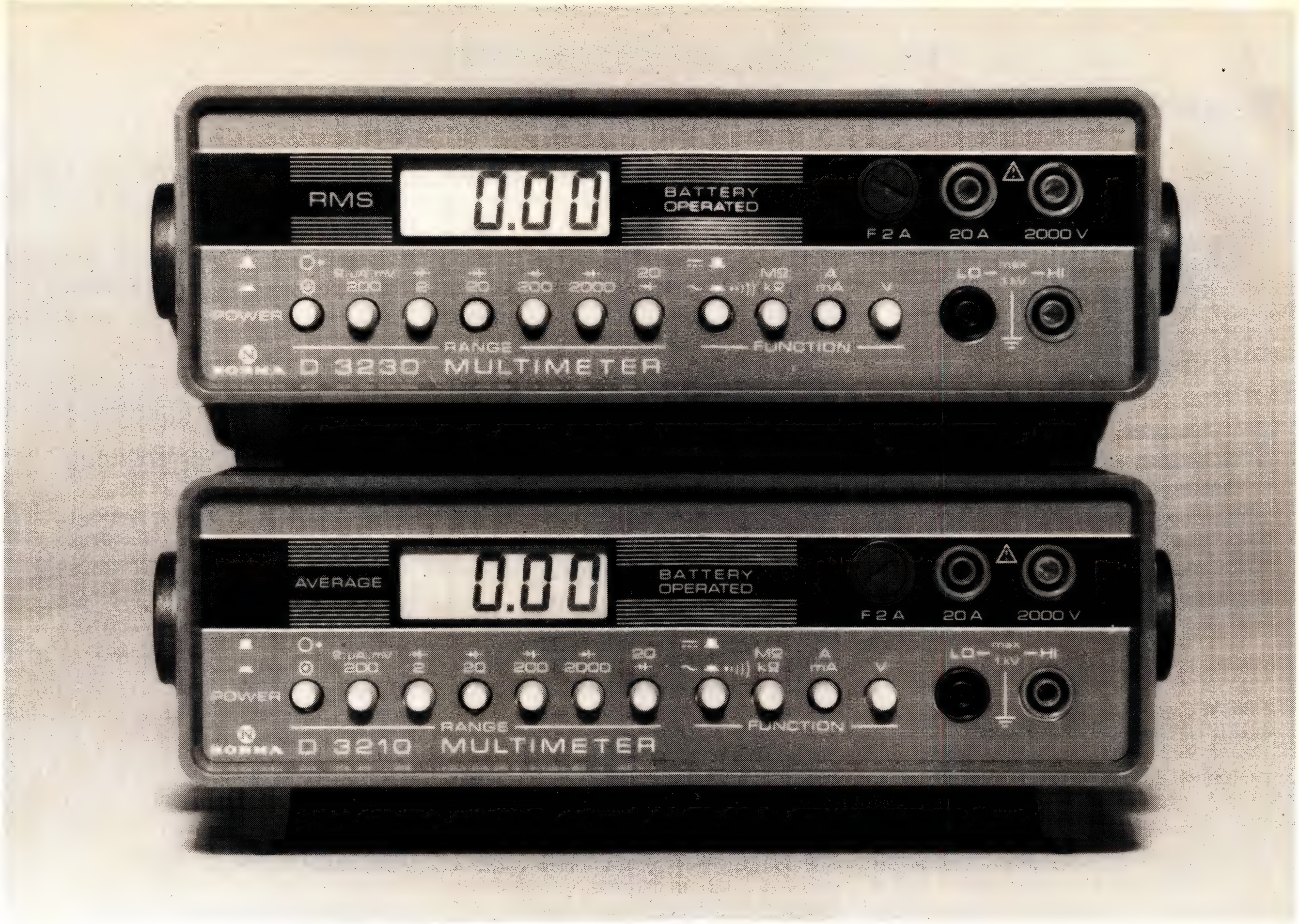
Circle 234 on reader service card



Two low-priced universal instruments: NORMA's MULTIMETER D 3210 and D 3230 RMS

The new MULTIMETERS D 3210 and D 3230 RMS are universal and reliable instruments. 10,000 resp. 2,000 hours of battery life ensure readiness of operation at all times – and they are sensationally low-priced.

Comprehensive ranges
Electronics and electrical engineering make increasing demands on meter ranges. The MULTIMETERS D 3210 and D 3230 RMS will measure currents up to 20 A, voltages up to 2000 V and resistances up to 20 megohms. A continuity tester with acoustical signal is also available.

Safety first
A perfect concept protects both the MULTIMETER and its operators from damage – even if mishandling or extreme loads should occur.

Analog output
A floating analog output permits connection of a recorder for graphic output of measured values.

Wide range of accessories
E.g. HF probe, HV probe and split-core transformer, for an extended range of applications of this versatile digital multimeter.

NORMA's successful multimeters

	DC AC	DC voltage AC voltage	Resistance
D 1216	2 mA–10 A	200 mV–1000 V	200 Ω–20 MΩ
	2 mA–10 A	200 mV– 750 V	
D 2210	20 nA–200 mA	200 mV– 600 V	2 kΩ–2 MΩ
	2 mA–200 mA	200 mV– 600 V	
D 2230	20 nA–200 mA	200 mV– 600 V	2 kΩ–2 MΩ
	2 mA–200 mA	200 mV– 600 V	
D 3210	200 µA–20 A	200 mV–2000 V	200 Ω–20 MΩ
	200 µA–20 A	200 mV–2000 V	
D 3230 RMS	200 µA–20 A	200 mV–2000 V	200 Ω–20 MΩ
	200 µA–20 A	200 mV–2000 V	
DA 3232	200 µA–20 A	200 mV–(2000 V)	200 Ω–20 MΩ
	200 µA–20 A	200 mV–(2000 V)	
D 4025	250 µA–2,5 A	250 mV–1000 V	25 Ω–25 MΩ
	250 µA–2,5 A	250 mV–1000 V	
D 4045 IEC 625	250 µA–2,5 A	250 mV–1000 V	25 Ω–25 MΩ
	250 µA–2,5 A	250 mV–1000 V	

A leader in meter design
New technologies, state-of-the-art design and more than 60 years experience in electrical measuring instrument manufacture combine to guarantee quality and reliability.

Worldwide sales and service network
Our sales organization is in touch with customers all over the world and ensures high workmanship in servicing. We export to 70 countries.

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NORMA – first in precision!

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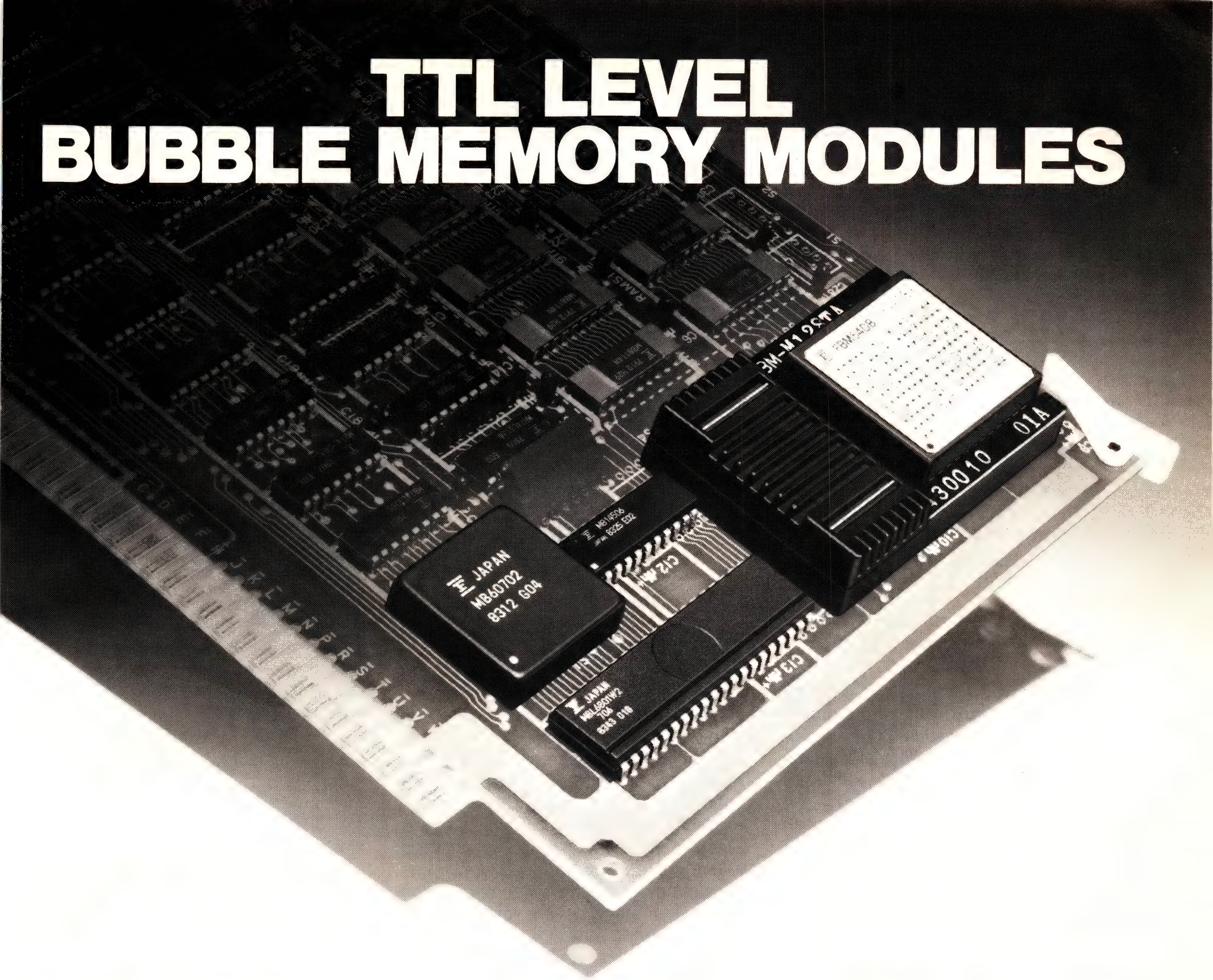
Circle 236 on reader service card

TTL LEVEL BUBBLE MEMORY MODULES



Fujitsu's BMM Series bubble memory modules let you design your own board.

Now you can have Fujitsu's reliable bubble memory just the way you want it. These flexible new modules, consisting of bubble memory devices and peripheral linear ICs, work at the TTL level which means you only have to add control LSIs to create solid-state file memory designed to your particular needs. Contact Fujitsu Component Europe, B.V. today for full details.

- Expandable from 128K to 4M bytes
- 11.2msec. average access time
- Non-volatile memory
- Maintenance-free design

Specifications

Model	FBM-M128TA	FBM-M128TC
Memory capacity	1,048,576 bits (128K bytes)	
Interface	TTL level	
Transfer rate	100K bit/s	
Access time	11.2ms	
Operating temp.	0 to 65°C	5 to 50°C
Storage temp.	−40 to 85°C	−30 to 75°C
Weight	75g	
Dimensions	43.5 x 65.5 x 13.7mm	

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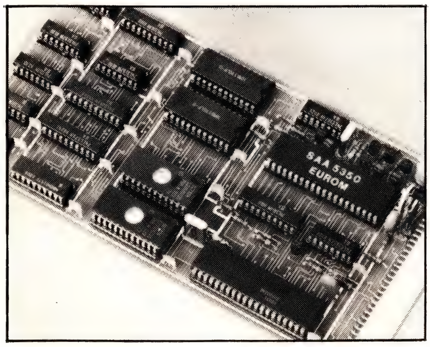
Circle 238 on reader service card

PHILIPS

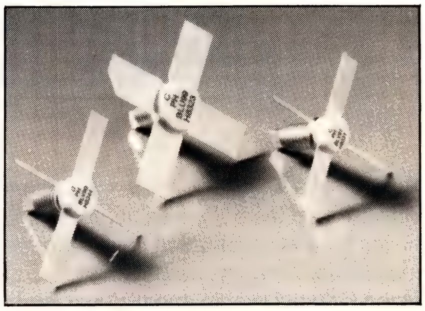
the complete component company

FIRST CEPT-COMPATIBLE IC FOR EUROPEAN VIDEOTEX MARKET

We announce the first-ever CRT controller IC to cover all the presentation level aspects of level 3 CEPT Videotex standard. Together with a suitable microprocessor and a minimum of only 4 K byte memory the new NMOS EUROM (EUropean ROM), type number SAA5350, allows the construction of a cost effective Videotex terminal. Data representing codes of the characters to be displayed on a TV screen is passed under microcomputer control to the SAA5350 (any 8- or 16-bit industry standard microcomputer will do). The SAA5350 includes timing chain, character generator, attribute logic, DRCS logic, video screen logic and microprocessor interface. The SAA5350 contains, in an on-chip 512 character ROM, all of the characters included in the ISO norm (ISO/MIS 6937/2) to cope with the 40 or so alphabets of Europe. The character shape is based on a character cell of 12 x 10 dot matrix to give a high-resolution, highly readable print-like display; double-height, double-width and double-size characters can be displayed. The IC contains on-chip block, smooth and line graphic shapes as well as DRCS logic, thus enabling high quality illustrations to be displayed on the TV screen. Up to 188 Dynamically Re-definable Character Set (DRCS) characters are supported by the SAA5350. These characters are downloaded to the terminal and stored in 2K bytes of page memory RAM. The DRCS allows the presentation of almost any symbol on the screen as every pixel in the 12 x 10 character cell can be defined by the data base; DRCS characters can be used for special symbols, diagrams, foreign alphabets and so on. The SAA5350 supports different DRCS formats which can be mixed at random on the screen. There are a total of 7 modes based on 12 x 10, 6 x 10 and 6 x 5 dot matrices. These modes allow choices between high-resolution monochrome display, and a lower resolution display which makes full use of the colour possibilities. The SAA5350 can display 32 colours per page, from a total palette of 4096 colours; it can decode and display characters at 13 different blinking speeds, and offers scroll facilities - an on-chip scroll map avoids the need for massive data transfer when scrolling. In addition to CEPT requirements, the SAA5350 also provides extra features for other applications, for example - 80 character/row option, multiple page memories, and full-screen DRCS. The SAA5350 is encapsulated in a 40-pin plastic package (SOT 129).



CIRCLE 273 ON READER SERVICE CARD



UHF POWER TRANSISTORS FOR MOBILE RADIO EQUIPMENT

Three new 12 V power transistors, the BLU99, BLV90 and BLV91 can operate in mobile radio equipment at either 470 MHz or 900 MHz. The transistors, designed for use in high gain common emitter circuits, are very reliable due to gold-metallised crystals based on microwave transistor technology. Multi-base structure plus diffused emitter-ballasting resistors ensure an optimum temperature profile and good zero-hour performance. The BLU99, a high gain successor to the well-known BLW80, is primarily intended as an output transistor in u.h.f. mobile communications systems but is also suitable for use at up to 1.2 GHz in amateur radio equipment. The BLV90/91 are driver transistors and ideal for use in cellular radio systems. The transistors come in a 4-lead ceramic capped stud envelope with all leads isolated from the stud; the BLU99 in SOT-122 and the BLV90/91 in SOT-172.

CIRCLE 274 ON READER SERVICE CARD

58 kW KLYSTRON COVERS 470 TO 860 MHz RANGE

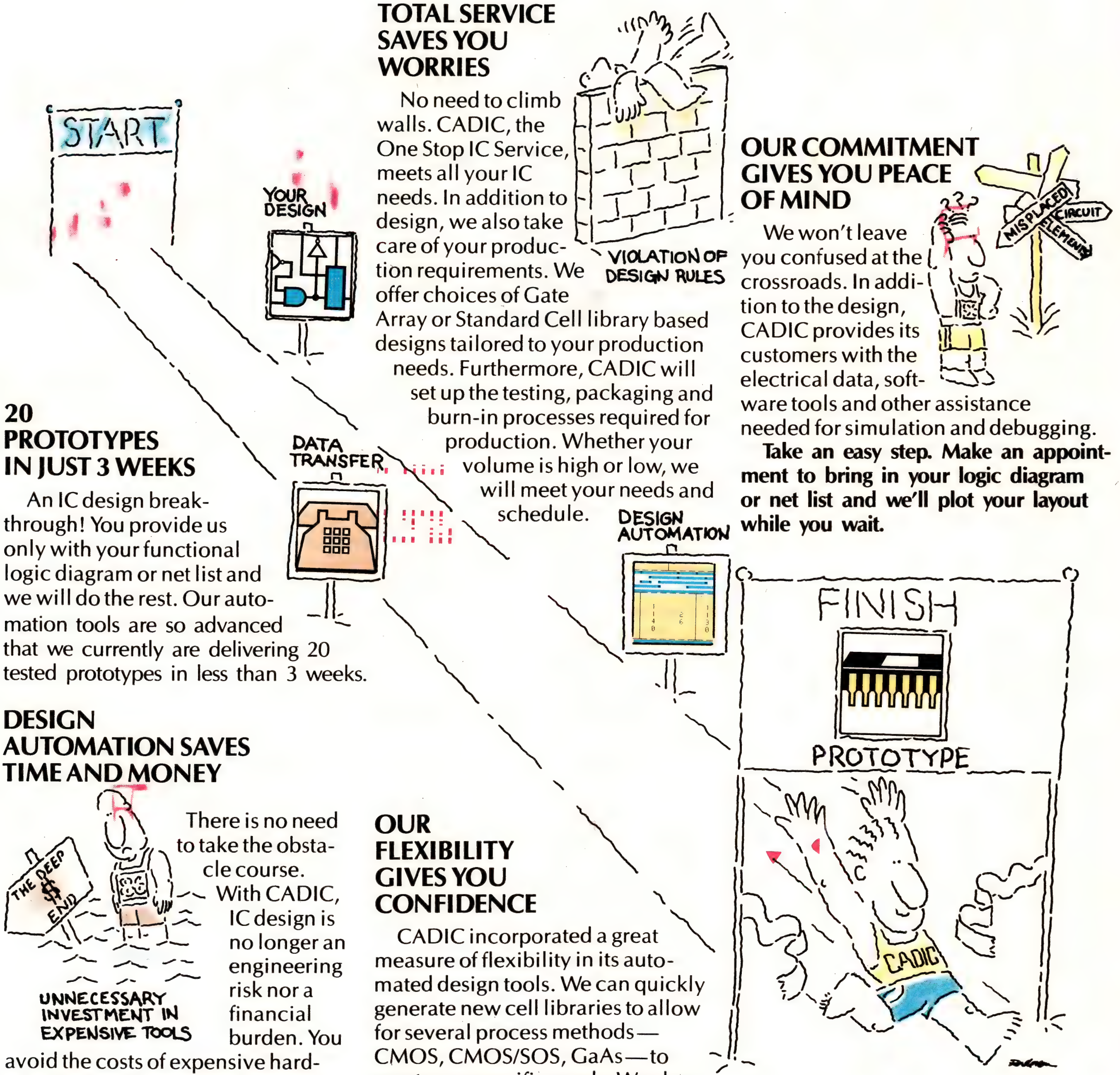
The YK1263 is a compact, highly efficient 58 kW UHF klystron that covers the complete 470 to 860 MHz frequency range for which formerly three conventional tubes were needed. Thanks to the compact design of the tube and its accessories, the complete assembly occupies an area of only 55 x 55 cm approx. (instead of the 80 x 80 cm of a single conventional tube). The air-cooled body design allows quick, easy installation and maintenance. The YK1263 has a gain of 40 dB, and is part of a new range of energy-saving klystrons with Annular Beam Control (ABC). In these tubes, a non-intercepting electrode is used to control the beam current. This ensures an adequate (but never excessive) current over the complete modulation range. ABC klystrons can operate at efficiencies of up to 65%, depending on the modulation circuits. The YK1263 has four external cavities, electromagnetic focusing and a high stability dispenser-type cathode. Beam data range from 23 kV/6 A for the lowest channel to 26 kV/4,85 A for the highest channel.

CIRCLE 275 ON READER SERVICE CARD

PHILIPS ELECTRONIC COMPONENTS AND MATERIALS DIVISON ☐ 5600 MD EINDHOVEN ☐ THE NETHERLANDS

PHILIPS

WANT TO GET 20 TESTED PROTOTYPES IN 3 WEEKS?


START
YOUR DESIGN
VIOLATION OF DESIGN RULES
MISPLACED CIRCUIT ELEMENTS
DATA TRANSFER
DESIGN AUTOMATION
FINISH
PROTOTYPE
CADIC
THE DEEP $ END
UNNECESSARY INVESTMENT IN EXPENSIVE TOOLS

20 PROTOTYPES IN JUST 3 WEEKS

An IC design breakthrough! You provide us only with your functional logic diagram or net list and we will do the rest. Our automation tools are so advanced that we currently are delivering 20 tested prototypes in less than 3 weeks.

DESIGN AUTOMATION SAVES TIME AND MONEY

There is no need to take the obstacle course. With CADIC, IC design is no longer an engineering risk nor a financial burden. You avoid the costs of expensive hardware and prolonged development. At the same time you make Marketing happy by introducing new products in a timely fashion.

TOTAL SERVICE SAVES YOU WORRIES

No need to climb walls. CADIC, the One Stop IC Service, meets all your IC needs. In addition to design, we also take care of your production requirements. We offer choices of Gate Array or Standard Cell library based designs tailored to your production needs. Furthermore, CADIC will set up the testing, packaging and burn-in processes required for production. Whether your volume is high or low, we will meet your needs and schedule.

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Announcing a new

16-Bit CMOS Microprocessor Strategy

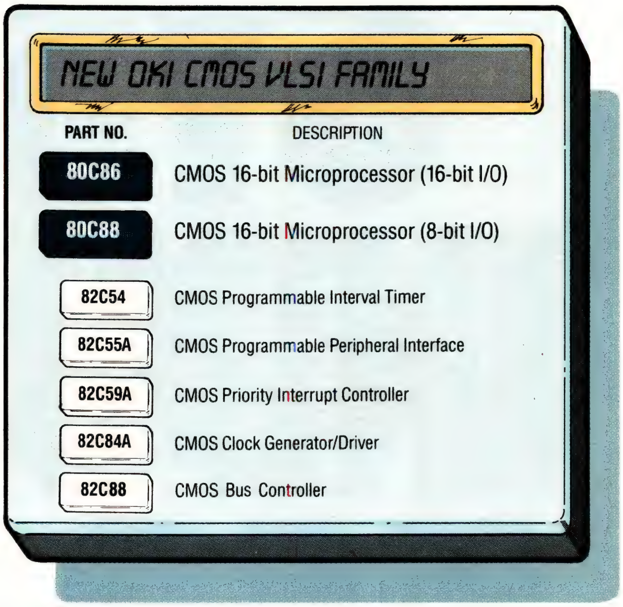
to assure the small-box designer total low-power system support.

OKI Semiconductor and Intel Corporation have announced an agreement to manufacture and market CMOS microprocessors, microcomputers and related peripheral circuits which are fully compatible with existing Intel devices. This cooperation will begin with the upcoming manufacture of the 80C86 and 80C88 16-bit microprocessor and peripheral family, using the OKI CMOS design now totally compatible with Intel's NMOS 8086/8088. Later next year, OKI will provide the power-down and bus-hold Intel version which is functionally identical as a replacement to the OKI design.

in CMOS!

What's in it for OKI 16-bit MPU users?

- **Easier application in standard NMOS designs:** The OKI CMOS design provides complete functional chip-compatibility with NMOS configurations: so totally compatible, absolutely no software changes are required.
- **Easier availability:** Reliability of supply is now improved by international second sourcing through two mutually-cooperative major IC suppliers—with availability scheduled in the second half of '84; qualification starting now.
- **Easier upgrade from 8-bit to 16-bit microprocessors:** Use your familiar 8086/8088 development systems without revisions or new capital investments.
- **Easier access to OKI robotized mass-production:** To handle worldwide volume demand, OKI in 1982 launched a further $360-million expansion of one of the world's most advanced, most automated semiconductor manufacturing facilities.
- **Easier packaging specification:** OKI's robotic technology can be programmed to accommodate a broad range of packaging options.
- **Totally safe to apply CMOS VLSI systemwide:** The freedom to utilize the power of CMOS throughout your small-box application is fully protected by OKI's license for worldwide merchant marketing.



NEW OKI CMOS VLSI FAMILY

PART NO.	DESCRIPTION
80C86	CMOS 16-bit Microprocessor (16-bit I/O)
80C88	CMOS 16-bit Microprocessor (8-bit I/O)
82C54	CMOS Programmable Interval Timer
82C55A	CMOS Programmable Peripheral Interface
82C59A	CMOS Priority Interrupt Controller
82C84A	CMOS Clock Generator/Driver
82C88	CMOS Bus Controller

Start the qualification process now for your upcoming portable small-system applications. Send for your data sheets today, and watch for the OKI Starter Kit announcement coming soon.

Send for Preliminary Data on the OKI CMOS 16-bit MPU Family

( ) Please rush technical information on the OKI compatible-CMOS MSM 80C86/80C88 Microprocessor Product Line.

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With PMDS II, you know the answer from the start.

- It is one of the most powerful development systems available
- It is universal
- It expands logically and economically to cover a wide range of applications (see table)

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More than universal

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Flexibility through UNIX*

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PMDS expansion possibilities

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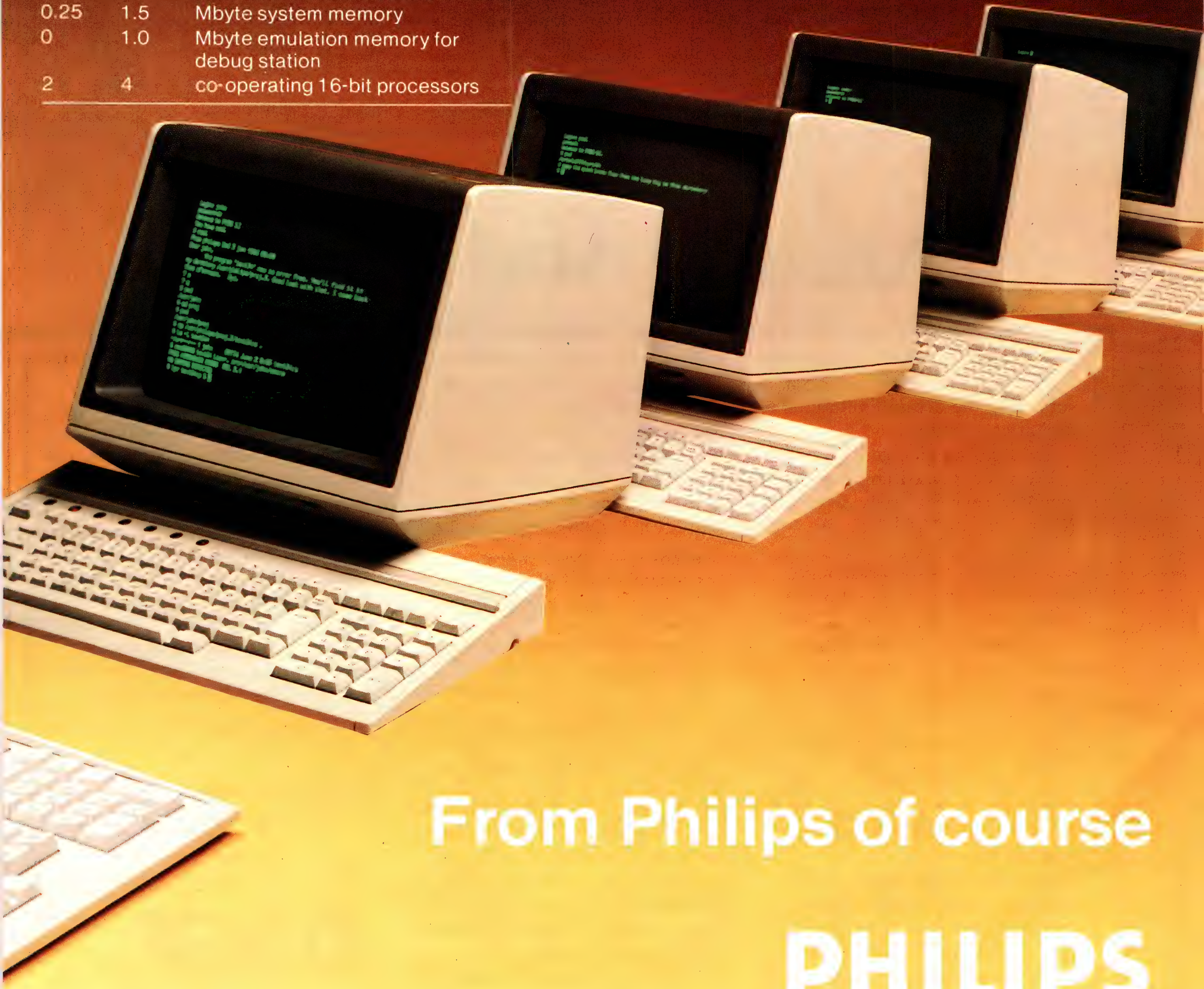
5	156	Mbyte formatted on-line storage
1	4	universal hardware debug stations
0.25	1.5	Mbyte system memory
0	1.0	Mbyte emulation memory for debug station
2	4	co-operating 16-bit processors



From Philips of course

PHILIPS

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GaAs ICs bid for commercial success

With speed the biggest attraction and materials improving, makers are planning to add capacity as start-ups seek backing

by Larry Waller, Los Angeles bureau

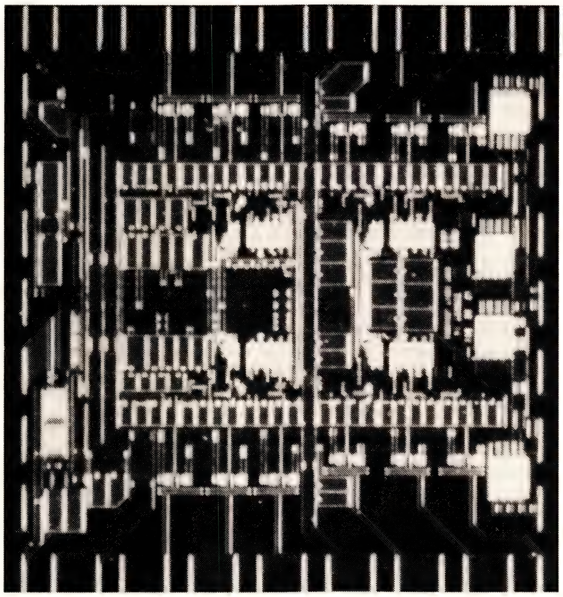
After nearly two decades of stop-and-go interest, gallium arsenide has earned a derisive billing: destined forever to remain the material of the future. But this III-V material, temperamental when compared with silicon, could finally begin to realize its high-performance potential if the recent flurry of activity maintains its momentum.

In fact, since Harris Corp.'s semiconductor operation in Milpitas, Calif., introduced the first commercial GaAs digital integrated circuits early this year, developments have come along briskly. Harris has two simple parts—a shift register and a binary counter—that are the first of a family. Their big feature is blinding speed—five times that of the fastest silicon equivalent.

This month, Gigabit Logic Inc., of Newbury Park, Calif., is to weigh in with a 12-member GaAs series, together with an evaluation board to simplify efforts to design with it. Japan's NEC Corp. is announcing its first commercial GaAs IC, a broadband intermediate-frequency amplifier in the 2-to-3-gigahertz range.

Moreover, many firms established to produce discrete GaAs field-effect transistors for microwave applications have dealt themselves into the IC game. Besides offering foundry services, these houses are busily developing chips and promise a stream of new ones in coming months.

No single reason for the upsurge stands out. Most often cited, however, is demand coming from the U. S. military, which seeks vast performance improvements for its systems by the late 1980s. Accordingly, a level of research and development funding that represents a high-water mark for support of gallium arsenide is already in the pipeline, with more in the offing. Systems work is under way, too, like the GaAs onboard satellite computer to be built by Raytheon Co., of Lexington, Mass.; and some semiconductor houses have contracts to deliver GaAs chips to defense-system builders.



Great gate. Gigabit Logic now offers a range of rapid gallium arsenide integrated circuits This quad three-input NOR-gate chip has a 75-picosecond propagation delay.

Next market. With the development steam generated by Government funding, these and other firms naturally are eyeing the commercial market. For example, at Tektronix Inc., "we recognized we had a technology with applications beyond our product line," says Al Patz, general manager for GaAs integrated technologies at the Beaverton, Ore., firm. Currently gearing up a GaAs foundry business split between military and commercial customers [*Electronics,* Feb. 9, p. 50], Patz believes that funding by the Pentagon is the major force behind the recent mushrooming growth but adds that the dollar tide will recede in two or three years. Tektronix' own debut will come late this year with a packaged depletion-mode gate array for foundry customers.

Companies that are intent on expanding their military foothold into the commercial IC market already number in the double figures. Rockwell International Corp.'s Defense Group, Anaheim, Calif., and Honeywell Inc., already fabricating memory and logic ICs at Richardson, Texas [*Electronics,* April 5, p. 164], are building a $16 million plant for the Defense Department, at Newbury Park. Also under construction is GaAs pioneer Varian Associates Inc., of Palo Alto, Calif., which plans a $16 million expansion of its Solid State Microwave division. Among others now tossing their hats into the ring are Avantek Inc., of Santa Clara, Calif.; Sanders Associates Inc., of Nashua, N. H.; and Adams-Russell Inc., of Waltham, Mass.

In a 1983 report, market research firm Strategic Inc., of San Jose, Calif., listed 42 companies with GaAs interests. But that is already out of date, admits Yves Blanchard, vice president of the semiconductor industry group. Strategic is racing to

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RAM (x8)	192	192	192	64	64
I/0 Lines	32	32	56	32	23
Serial Comm.	UART	UART	UART	—	—
Counters	2 x 16	2 x 16	2 x 16	1 x 16	1 x 16
Expansion Bus	65K	16K	16K	—	4K
Interrupts External Internal Host	 6 4 —	 6 4 —	 6 4 —	 3 1 —	 4 1 2
Standby RAM (mW)	12	12	12	35	—
Package	64-pin QUIP	40-pin DIP	64-pin QUIP	40-pin DIP	40-pin DIP
Replaces	8031	8051		8048/49	8041

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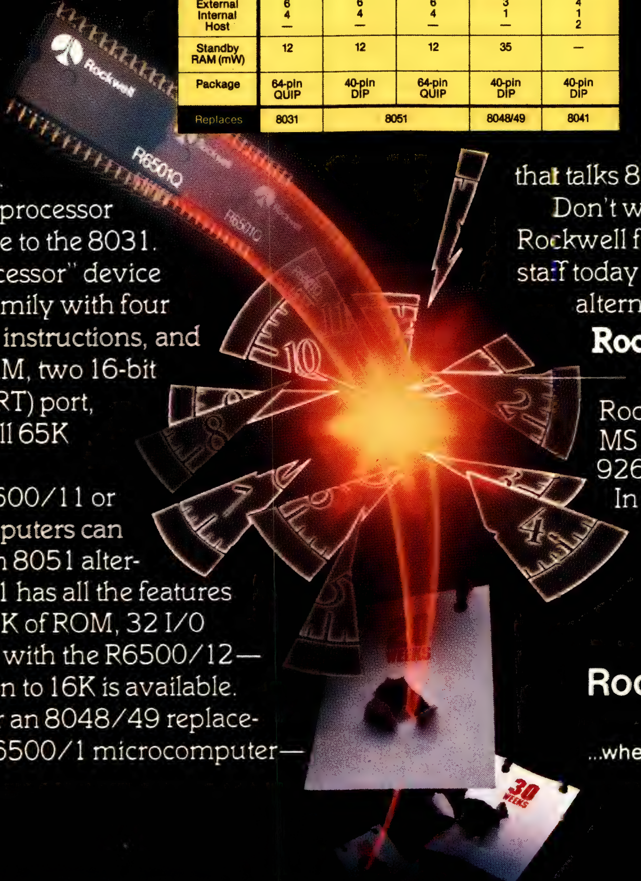

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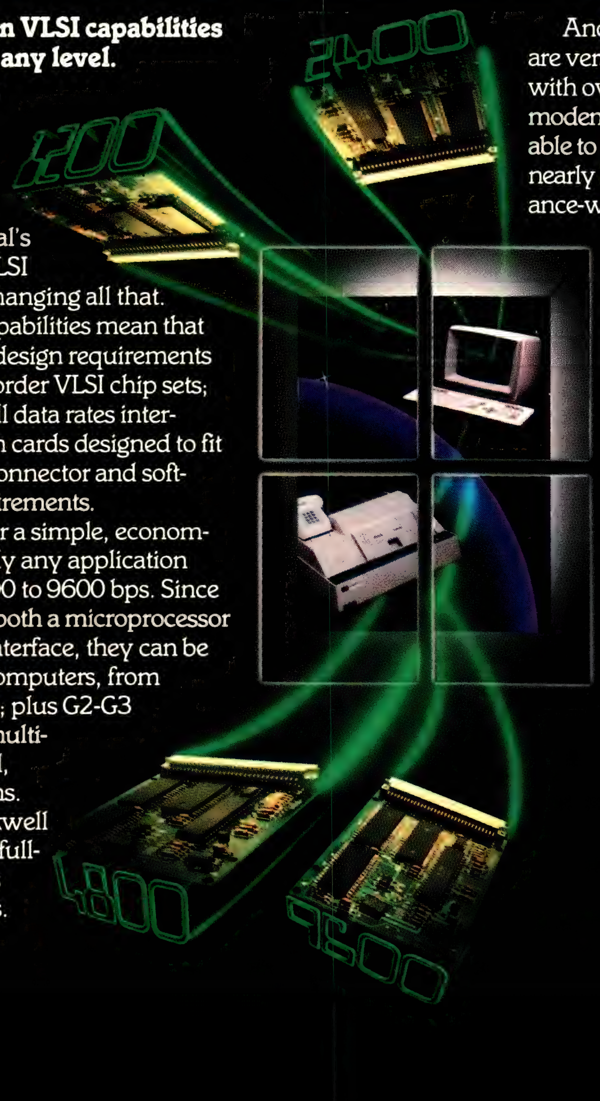

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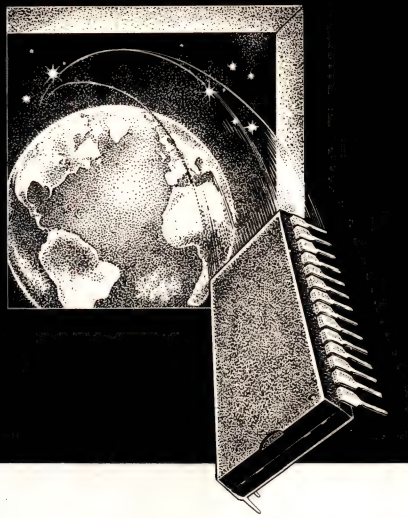

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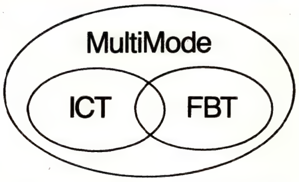

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Government

Aging software swamps bureaucracy

Despite years of heavy outlays intended to upgrade obsolete software, Washington's bill for software maintenance will reach $9.8 billion by 1990

by Karen Berney, Washington bureau

"Breakthroughs in both technology and management are needed to turn the tables on the biggest automation problem facing the Federal government." That is the word from Warren Reed, director of the General Accounting Office's Information Technology and Management Division, who like many Federal information-processing officials, finds much to fret about in the Government's overage software inventory.

But no major improvements are expected soon. At the beginning of the decade, Washington was spending $200 million annually to modernize old software. That figure will climb to $2.1 billion by 1990, reports the Office of Management and Budget. Maintenance costs—another measure of the problem's dimensions—will also jump more than tenfold to $9.8 billion during the 1990s. That will account for about 43% of total Federal expenditures on software, notes the OMB.

Causes and cures. Understanding how the Government got into such a mess is easier than figuring a sensible way to get out of it. Essentially, it got involved with data processing too early for its own good—long before data-processing and management software was an off-the-shelf product, explains Francis A. McDonough, deputy assistant administrator for information resource planning at the General Services Administration.

For that reason, the Government had to design about 95% of its application programs in house. These now total over 5 million packages running on some 17,000 machines. "While we can justify replacing antiquated, rundown hardware, we can't simply scratch a 20-year investment amounting to hundreds of staff years to design, test, and install software," McDonough contends. Not only are the costs prohibitive but so is the impact on people. The trauma both users and programmers undergo when dealing with a totally new system is so severe that managers tend to avoid changes, he says. The upshot is that nearly every Federal agency is saddled with some degree of obsolete software.

In the inventory, programs written in assembly language and Cobol 68 predominate. These languages were not designed for flexibility, which makes migration to new hardware "a very mean job," says McDonough. Moreover, since they were neither well documented (only 40% of the inventory has been recorded) nor well written, Federal data-processing facilities are in a perpetual state of crisis referred to as "unscheduled maintainence." Such is the magnitude of the problem that the U. S. Air Force estimates that it would need up to 25% of all the country's 18- to 24-year-olds by the year 2000 to keep its software up and running—should the software problem go unchecked.

It could have been otherwise. As an early starter, Washington had a grand opportunity to stay one step ahead of technology, observes Phillip Kiviat, vice president of government operations for Sage Systems Inc., a Rockville, Md., supplier of software development tools. "They [the Government] simply blew it," he claims.

Missed opportunity. Had Federal managers had the foresight to invest enough to keep their systems current, the Government would be a leading user of new data-processing techniques, Kiviat maintains. Instead it became an institution frozen in time, he insists.

But Richard Harrison, director of the GSA's Federal conversion support center, counters that "private industry is not better or worse off than the public sector. Any large organization with large inventories to maintain is bound to be experiencing software

THE TOP 10 U.S. AGENCY BUDGETS FOR INFORMATION PROCESSING TECHNOLOGY
($ MILLIONS)

Department or agency	Fiscal 1985	Fiscal 1986	Fiscal 1989	Total 1985–1989
General Services Administration	1,083	1,754	1,295	6,619
Army	646	705	635	3,287
National Aeronautics & Space Administration	522	567	537	2,776
Air Force	533	442	497	2,291
Navy	468	531	404	2,253
Treasury	263	295	334	1,546
Justice	232	239	210	1,095
Agriculture	248	330	135	1,093
Energy	128	216	113	845
Health & Human Services	189	152	91	672

SOURCE: OFFICE OF MANAGEMENT AND BUDGET

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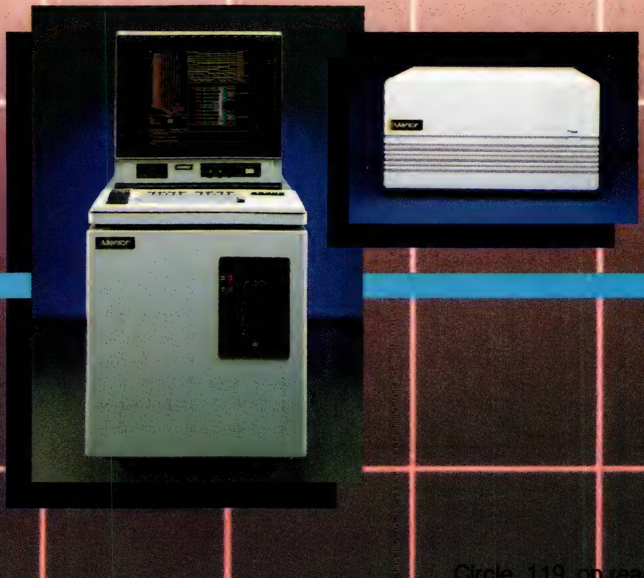

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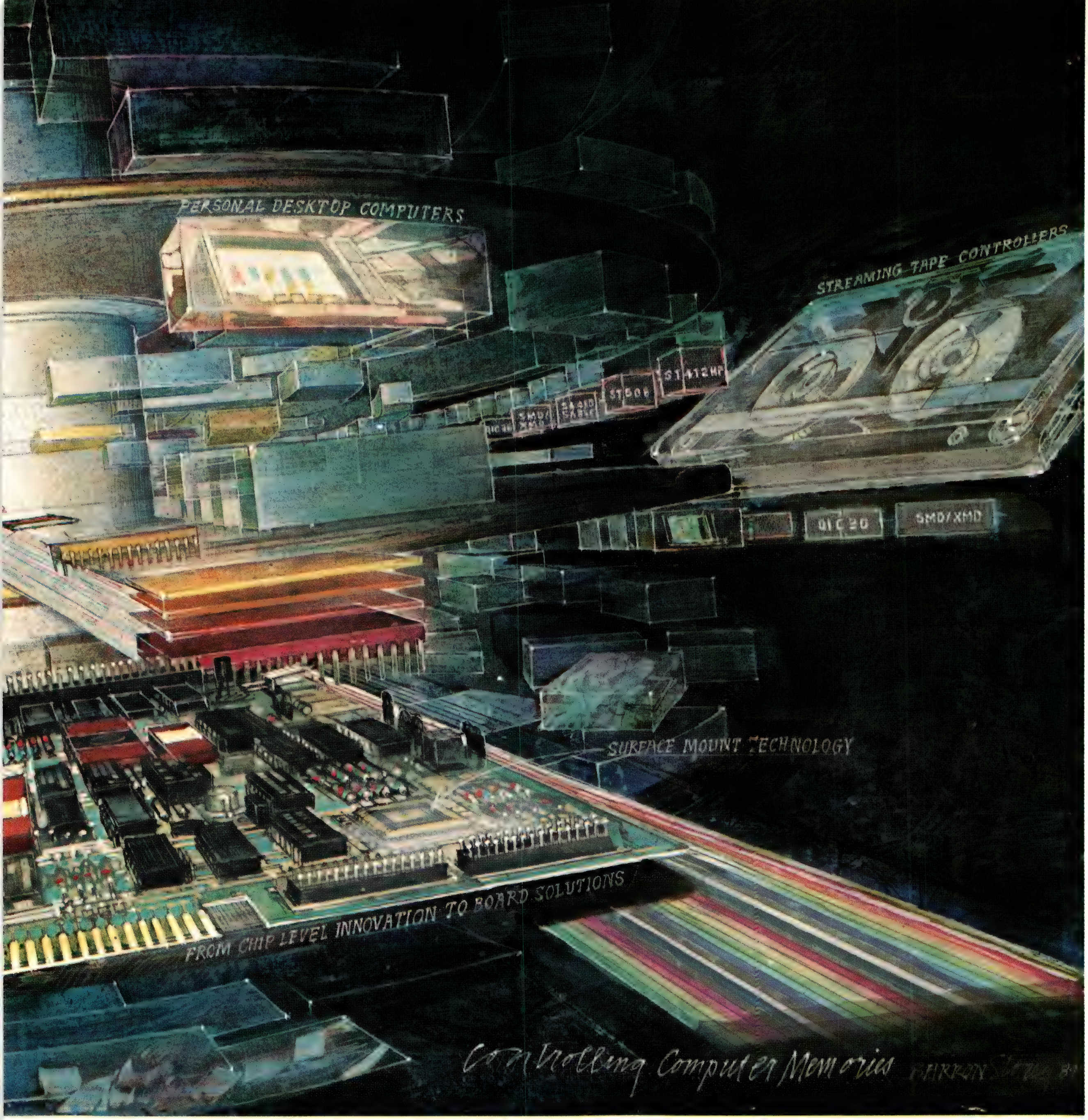
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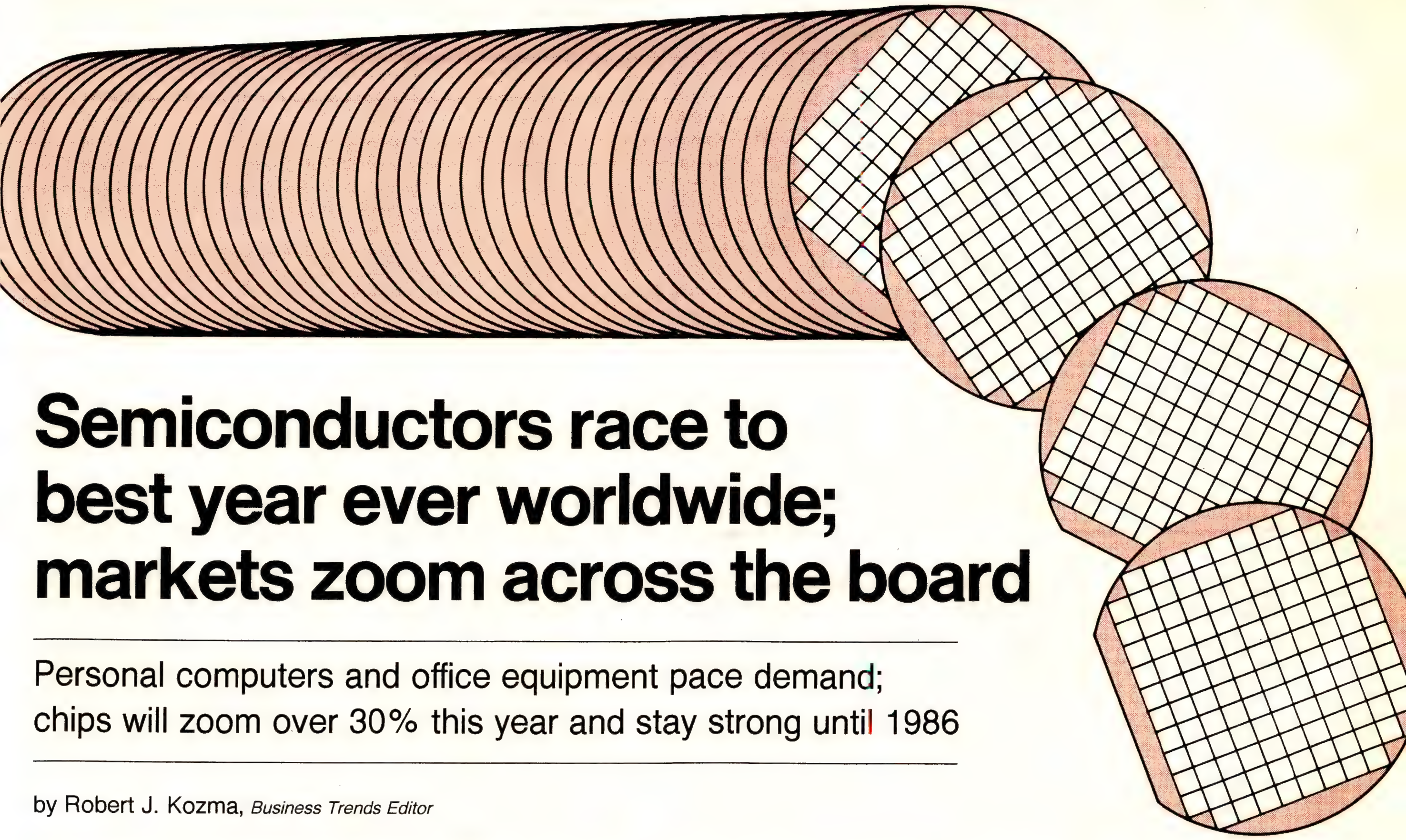


Semiconductors race to best year ever worldwide; markets zoom across the board

Personal computers and office equipment pace demand; chips will zoom over 30% this year and stay strong until 1986

by Robert J. Kozma, *Business Trends Editor*

☐ It's double thumbs-up for silicon shapers around the world, as the now-global recovery has set equipment manufacturers off on a semiconductor buying spree of unprecedented proportions. Industry watchers see worldwide business climbing well over 30% this year and continuing strong until 1986.

In 1982, the semiconductor industry underwent a mini-recovery, only to see its hopes for continued good times dashed under the heels of the lingering recession. In 1983, the industry again saw orders increase, leaving executives to wonder if the springtime rise in business activity signaled the long-awaited upturn or merely presaged a repeat of the previous year's frustration. This year, everyone knows for sure: business is booming.

The Semiconductor Trade Statistics Program (STSP) of the Semiconductor Industry Association, in San Jose, Calif., forecasts that semiconductor shipments by U. S. and European chip vendors will total almost $15.2 billion, an increase of 37% over 1983 shipments of just over $11.0 billion. The STSP sees this growing another 24% next year, to almost $18.9 billion, with a 1986 U. S. and European projection of another 19% growth, to $22.4 billion (Table 1). As for Japan, market researcher Dataquest Inc., San Jose, predicts that its market will grow 37% this year, to $7.7 billion, compared with the 1983 market of $5.6 billion, and climb another 25% in 1985.

"Cycles [of expansion in the semiconductor business] tend to last for four years," observes Daniel L. Klesken, a market watcher with Montgomery Securities, San Francisco. "We're only five quarters into [this one], which means there's still 10 to 13 quarters ahead of us." Klesken projects growth in 1984 of 45% to 50%, versus 25% growth last year. The leading U. S. manufacturers could do even better (Table 2). "This is the strongest growth ever for the industry on a year-to-year basis. I'm very optimistic," he says, adding that he thinks the industry will grow to $45 billion by 1989, from $23 billion last year. Industry executives say business is over for 1984—everything the industry can or will make for the remainder of this year is essentially claimed by equipment manufacturers around the world—and eyes are now turned to 1985.

Demand continues to come strongly from makers of personal computers, the same market that started the semiconductor industry on its current road to prosperity last year. "The problem is PC-itis," notes Leslie L. Vadasz, senior vice president of Intel Corp., Santa Clara, Calif., referring to the phenomenal growth of the personal-computer industry in the U. S. and overseas. "There's no question the personal computer has added tremendous volume demand on the semiconductor industry." Klesken estimates the personal-computer industry, which was just in its infancy in 1977, this year will gobble up 10% of the worldwide semiconductor market.

But manufacturers of products other than the personal computer have made their presence felt in the semiconductor market, as the recovery—now in its expansionary phase—moved to other parts of the U. S. economy and as conditions got better overseas. Thus, demand for chips by manufacturers of minicomputers, office-automation

Deregulation, move to digital technology pace telecom-chip market

The story of the market for telecommunications chips is a tale of two factors of growth, says Ronald R. Ruebush, group product marketing manager of telecommunications devices for Advanced Micro Devices Inc., Sunnyvale, Calif., In the central-office area, the growth rate usually tracks the increase in the number of phone lines and may be a little more than 5%, he says. "But what you are also now seeing is the conversion of the existing base into the digital [technology] from the previous generation of analog technology. Because of that [development], the actual annual growth rate is probably on the order of 35% to 40%."

The movement to digital switching is not a result of last year's recovery, says Ruebush. Rather, it results from long-range plans to upgrade central offices. More than half of that market is in Europe, where government-funded programs fuel the change, he notes.

Driven by "the major state of technological change," Ruebush says, digital-switching components—such as AMD's AM7901 subscriber-line audio-processing circuit [*Electronics*, May 5, 1982, p. 113] and companion AM7950 subscriber-line interface circuit—are moving into volume production and deliveries in a big way. The digital-switch market is also seeing a lot of activity from private-branch-exchange makers rushing to provide computer data and voice communications.

Besides the movement to change the installed base from analog to digital technology, the breakup of American Telephone & Telegraph Co. and phone deregulation caused an explosion in the telecommunications customer base. Hundreds of firms are now making everything from switching systems to consumer phone units, notes Randy Hutcheson, product planning and applications manager for Motorola Inc.'s Logic and Special Functions division, Austin, Texas. Last summer, some operating companies began dealing heavily with independent non-AT&T suppliers; that "quick snap took the industry a little by surprise," Hutcheson says. The sudden change in buying habits caused a surge in demand for Motorola's single-chip codec-and-filter MC14403 [*Electronics*, Jan. 27, 1982, p. 146].

Modems, which are riding the coat-tails of the hot personal-computer industry, are growing in the 24% range, estimates Al Mouton, product planning section manager for Motorola. Overall, he sees the total available market growing from $155 million to $2 billion by 1989.

Motorola believes it has 60% of the low-speed (300-baud) modem market. It is serving this consumer market with both a single- and a two-chip modem. About 1.5 million 300-baud modems were shipped last year. A major battle in the voice-data PBX arena has been shaping up, with computer firms teaming with switching houses. This, of course, will provide some business for telephone-chip makers.

Mostek Corp., Carrollton, Texas, also hopes to capitalize on the changes taking place in the communications industry, as the firm moves from its base of codec, filter, and dialer chips into new data- and voice-transmission markets, says Jim Garrett, marketing manager of communication products. This includes the two-chip Ethernet interface that it worked on with AMD [*Electronics*, Oct. 6, 1982, p. 92]. Mostek's main contribution to the effort is the MK68590 local-network controller. The second chip is a bipolar serial interface adapter. The two firms are looking at other chips to combine voice and data—such as X.25 point-to-point links using codecs for voice. Mostek communications chip managers believe the networking milieu is still unsettled as to which of the various telecommunications standards will dominate in which markets. **—J. Robert Lineback**

Intel president Andrew Grove recently joked that supply would catch up with demand "during the next recession, and they'll be in balance for 37 minutes."

The rush to add new manufacturing capacity, however, may present problems for the industry in the future. "Everybody's running like hell [to add capacity] so they don't lose market share," notes James L. Barlage, who keeps tabs on the semiconductor industry for Smith Barney Harris Upham & Co., New York. He argues that putting a total on the amount of chips that the industry can produce is difficult because of the variance in the number of shifts worked per plant and the yields per wafer. The industry is currently running at a rate of about 70%, he estimates.

Capacity versus demand

"I think [the industry] will have a difficult time keeping capacity in line with demand," Fairchild's Brooks adds. "When the economy turns, we'll have a massive correction." That is, the change from good times to bad when all the capacity comes on line will be as sudden as when orders went from bad to good in 1983.

Today, for many manufacturers, "the name of the game now is managing bookings," so that double-ordering and over-booking can be held in check, notes Michael H. Graff, vice president of sector marketing, Harris Corp., Melbourne, Fla. Texas Instruments Inc., Dallas, among others, has been doing that by matching its projected production capacity with promised deliveries. The computer-based allocation program is designed to guarantee that at least 90% of TI's deliveries will be on time—something that the firm hopes will calm customer's fears in these days when demand outpaces industry capacity, says Tom Balch, marketing manager for digital bipolar commodity products.

"While we do not have a lot of evidence of double booking, we do think there are competing system products in a number of areas where manufacturers are collectively going for much more than 100% of the market share," notes James R. Fiebiger, vice president and general manager at Motorola Inc.'s Semiconductor Products Sector, Phoenix. Semiconductor makers are generally becoming more concerned about the sales expectations of semiconductor buyers, he adds.

Intel "caused some buying panic" when it initiated a bookings-control system, notes Jack C. Carsten, senior vice president of the firm's components group. Intel stopped accepting orders for some products "for six

Electronic Components and Materials division. "We see a tremendous pickup in the market." (Fig. 2)

The Philips executive sees business in some TTL lines as hectic and says there is a worldwide shortage. Such a shortage also exists in microprocessor chips, while in memories and standard logic, "business is fantastic, and standard complementary-MOS is going like hell," Holtwijk proclaims. Both the consumer, and especially the professional, sectors are growing, he adds.

In the professional sector, three factors spell big business for TTL and ECL lines: the lively personal-computer market, particularly in the UK, and respectable sales of mainframe-computer and communications equipment throughout virtually all Europe.

Taking a broader view of what is fueling the big push in IC sales, Holtwijk cites three prime factors. First, there is the overall growth in gross national products in the industrialized countries of the West, and IC sales tend to follow the GNP. Second, new IC applications, such as personal computers and the addition of text display and processing to TV sets, are coming up, coupled with ICs' greater penetration into existing equipment. Finally, ICs are replacing more conventional electronic components.

Holtwijk predicts further growth: "I am convinced that IC sales will spurt at an average rate of at least 20% a year through the end of this decade." He points out that as a result of economic recessions that are likely in the future, the growth in some years may fall below the average. But that will be made up by years when the industry achieves year-to-year growth of over 40%, although not all observers are so optimistic about the continental market (Table 4).

As for the chip business in the UK, growth rates for the overall semiconductor market in 1984 will be up 40%, according to Texas Instruments Ltd., Bedford. Britain, which once had no participants in the market for high-volume standard semiconductor products, now has two. One is the National Enterprise Board-backed Inmos Ltd., Bristol; the other is STC Semiconductors, a division of Standard Telephones and Cables plc, London, under largely UK ownership since ITT Corp. partially divested itself of its UK subsidiary. And a third is on the way—a start-up called Integrated Power Semiconductors Ltd.

TABLE 3: MAJOR EUROPEAN IC PRODUCERS

Manufacturer	(IC production millions of dollars)		1983 – 84 % increase
	1983	1984 (forecast)	
Philips*	250	300	20
Siemens AG	200	260	30
SGS-Ates	175	260	49
ITT Corp.	100	135	35
Ferranti Electronics Ltd.**	75	125	67
Thomson-CSF	60	75	25
Inmos Ltd.	57	150	163
Plessey Co.	50	65	30
AEG-Telefunken	40	50	25
Others	43	60	40
Total	1,050	1,480	41

*Not including Signetics **Not including Interdesign

SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

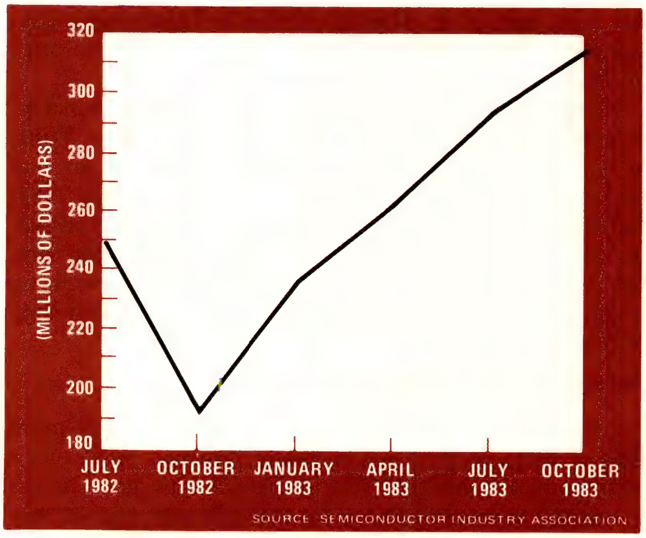
Inmos's place in Britain's industrial ranks is far from assured, mostly because it has not arranged the cash for its ambitious plans. In recent months, several large firms have looked it over—among them Britain's General Electric Co. plc and American Telephone & Telegraph Co. None seems interested in Inmos's business strategy, though all envy its very-fine-line production setup.

Second-largest MOS maker

The company claims to be on target, having made a profit of $1.85 million on a turnover of $28 million in the first quarter of 1984. As its Newport, South Wales, facility ramps up, it expects to reach a $140 million annual turnover with profits of around $10 million to $14 million this year. This will likely make Inmos Britain's most extensive operation for very large-scale integration. Already, according to Dataquest, the firm is Europe's second-largest MOS manufacturer, behind Philips.

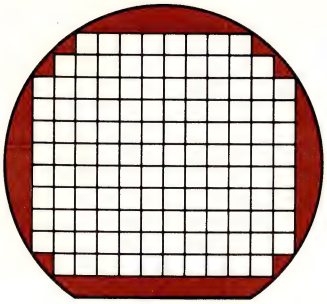
The company also is pushing ahead with its strategy of focusing on leading-edge high-performance parts. For example, it decided to implement its 32-bit transputer processor [*Electronics*, Nov. 17, 1983, p. 109] in C-MOS technology to avoid problems of heat build-up and will base all its future memory products on that technology. The first of these parts, due in the fourth quarter, will be a high-performance 64-K static RAM, slated for high-performance uses in supercomputers, telecommunications, radar, and signal-processing applications. Also planned for later this year is a 256-K C-MOS dynamic RAM.

The transputer—the initial samples of which will be available late this year—continues to excite interest in companies as diverse as mainframe and minicomputer maker ICL plc and personal-electronics manufacturer Sinclair Research Ltd. The groundwork is also being laid for integrating the transputer into a variety of chip products, beginning with a disk-drive controller and following with a graphics controller. Moreover, a silicon-systems group will produce standard parts as well as custom versions for big manufacturers.



SOURCE: SEMICONDUCTOR INDUSTRY ASSOCIATION

2. Taking off. Orders booked by European chip makers, after falling to $192 million in October 1982, rose as the economic recovery in the U. S. moved overseas. By October 1983, the last month for which data is available, bookings had reached $316 million.



Japan boasts strong market with vendors rushing to fill buyers' needs worldwide

☐ The market for semiconductors in Japan, like the markets in the U. S. and Europe, is exceptionally strong, with most major chip houses experiencing over 50% growth in production (Table 5) and still not satisfying all their customers. "In the past, we have had shortages of microprocessors, TTL, and other devices, but nothing on this broad a scale," notes a semiconductor executive at Fujitsu Ltd., Tokyo, who declined to be identified. "Virtually every category is in short supply. We're working weekend shifts to keep up with demand."

Manufacturers may have to continue scheduling those weekend shifts. According to Dataquest, Japanese consumption of semiconductors this year is expected to grow 37%, to about $7.7 billion, compared with 1983 chip consumption of $5.6 billion. Growth in 1985 for Japan's domestic semiconductor market will be another 25%, Dataquest projects. Shortages exist for such products as TTL parts, 16-K and 64-K static RAMs, dynamic RAMs, MOS logic, microcomputer peripherals, and codecs.

"Semiconductor growth is crazy," exclaims Tsuyoshi Kawanishi, group executive of Toshiba Corp.'s semiconductor group, Tokyo. "Japan's GNP growth is 4%, the electronics industry's growth is about 12%, and IC growth is 36% or more." Toshiba's semiconductor sales have increased 57% from a year ago, he adds.

"Why is electronics growth three times that of the GNP?," Kawanishi asks rhetorically. "Electronics is becoming the main industry in Japan," he replies, citing robust growth in video cassette recorders, other consumer-electronics products, and office-automation markets. The semiconductor industry is growing three times faster than the overall electronics industry because "electronics is becoming semiconductors. You open the [piece of electronics equipment] and it contains mostly semiconductors—terminals and television sets, for example, are ICs and a picture tube. Furthermore, systems are becoming more complex, so a moderate increase in equipment sales translates into a large increase in semiconductor sales."

Information processing leads surge

Growth is strong in the information-processing industry, especially from personal-computer manufacturers, which have exploded in number, and office-automation-equipment makers. In fact, semiconductor suppliers are worried that too many personal-computer vendors are trying to capture parts of the market. "Depending on the specifications, price, and timing of a new product announcement, the manufacturer [of a personal computer] either has a hit or a product that can't be sold," observes Hisao Kanamaru, manager of the marketing and planning department at Hitachi Ltd.'s Electronic Devices group, Tokyo. "This makes for confusion in the semiconductor market," since personal-computer vendors will have already placed orders that either will be not needed or not large enough.

Kanamaru estimates growth in office automation (including personal computers, word processors, and office work stations and computers) in the 25%-to-50% range. That is fairly significant, since observers say these products account for about 30% of the semiconductor industry's output—especially microprocessors, memory, and TTL parts.

In consumer electronics, Japanese vendors are building and shipping VCRs to markets around the world, and that is squeezing Japanese chip suppliers. For example, VCRs usually use 4-bit microprocessors, linear ICs, and logic chips, sources note. However, as one executive points out, "there is a constant need to add new features to meet competitive pressures, but there isn't time to design new custom ICs, which takes perhaps six months. The same functions can be realized using small-outline-package transistors, which fuels the demand for a great number of transistors." With output of VCRs expected to reach 26 million units this year from 18 million last year, and with each VCR using an average of over 150 discrete transistors, it is no wonder that supplies are tight.

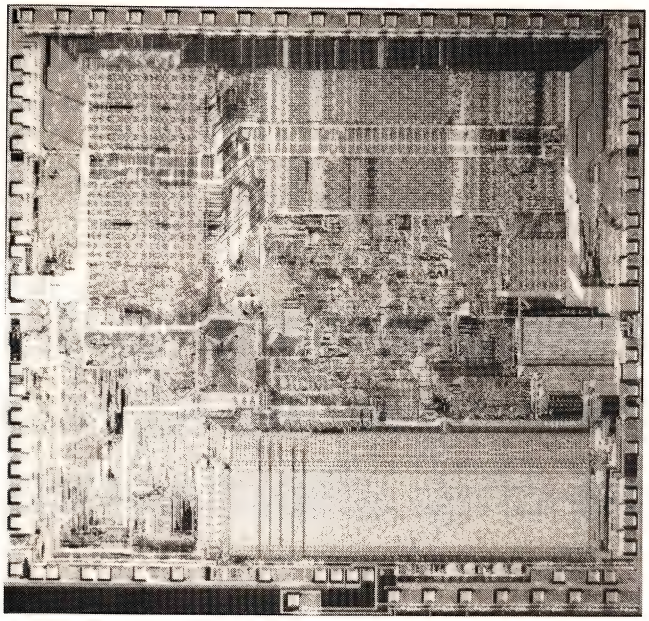
The communications market, which is about 10% of the Japanese semiconductor market, is described as having flat growth now. But that might turn to dynamic growth in the future, depending on the implementation of new telecommunications laws that are due to take effect April 1. One of these would turn Nippon Tele-

TABLE 5: TOP JAPANESE IC PRODUCERS

Manufacturer	(IC production* millions of dollars)		1983 – 84 % increase
	1983	1984 (forecast)	
NEC Corp.	1,040	1,575	51
Hitachi Ltd.	800	1,255	57
Toshiba Corp.	600	975	63
Fujitsu Ltd.	500	775	55
Matsushita Electronics Corp.	310	510	65
Mitsubishi Electric Corp.	295	475	61
Tokyo Sanyo Electric Co.	230	370	61
Oki Electric Industry Co.	220	365	66
Sharp Corp.	175	250	43
Sony Corp.	70	110	57
Others	180	290	61
Total	4,420	6,950	57

¥235 = $1.00 *Based on calendar-year estimates and not including hybrids.

SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.



3. Battlefield. The combination of Texas Instruments Inc. with National Semiconductor Corp. to jointly develop National's 32032 family of 32-bit microprocessors promises to tighten up the race for dominance in this important product market.

a 32-bit microprocessor to market and that Motorola, which he classifies as a strong No. 2, will not be able to catch up. Both firms and their competitors are aiming to grab market share with new state-of-the-art products.

"Everyone wants one work station on their desk" to perform a plethora of tasks, notes Dave House, vice president and general manager of the microcomputer group at Intel. He says manufacturers are using a 68000 chip for high-speed computational uses but are adding an 8086 to run IBM Corp. Personal Computer software. "The iAPX 386 is aimed at that market, replacing two chips [Motorola's and Intel's] with one chip," House maintains.

Motorola, for its part, continues its plans to introduce the much-awaited 68020 32-bit microprocessor this summer, which will have greater interprocessor-communications ability than the present high-end, the 68010. This processor will play a factor in the design of new systems architectures that divide up tasks among several processors. Already, the 68010 is finding its way into quite a few fault-tolerant systems because of its speed and an instruction set that allows it to suspend a task and hand it off to another 68010 for completion.

Motorola executives claim that reports by market researchers say 7 out of 10 equipment designs in Japan are being won by 68000 chips. That is a major shift from a year ago, they say, when Intel's 8086/88 chips were winning designs on the strength of their use in IBM's PC. Motorola believes its second-source strategy is beginning to pay off in a big way. It has a half dozen second sources—one of which is in Japan while two others are in Europe.

'Most important new product'

National Semiconductor's unveiling of the 32032 microprocessor (Fig. 3) was "the most important new product introduction our company has had," says president Charles E. Sporck, adding that success with the 32-bit line "exceeded our expectations." Says Smaha, "We feel we're in a strong position with our 32-bit product line. We're having very good success with design wins."

TI's decision to hook up with National to develop additional products within the 32-bit family does not mean that the Texas firm is abandoning its niche-market strategy. While TI executives are enthusiastic about their future efforts with National, they are equally enthusiastic about dedicated processors. This application-specific microprocessor market includes such products as TI's TMS 320 digital-signal processor, which has broken the firm's record for first-year sales by a microprocessor. Other promising areas for application-specific microprocessors include graphics and local networks.

TI believes that these microprocessors must be based on new architectures, not tied to a central-processing host family, says James Huffhines, manager of business development in TI's programmable products division, Houston. That was the case with the signal processor and will be the case with TI's local-network processor.

Offering microprocessor products for niche markets is a strategy that Donald W. Brooks, executive vice presi-

Demand for 64- and 256-K RAMs to jump this year

Worldwide demand for 64-K dynamic random-access-memories tripled in 1983, reaching 340 million units, according to Texas Instruments Inc., Dallas. William N. Sick, executive vice president of TI's Semiconductor Group, estimates that 64-K demand this year will be in the range of 750 million to 800 million units. The company is predicting that 64-K volumes will peak in 1986 at 1.2 billion units.

In the emerging 256-K RAM arena, TI estimates that 20 million to 25 million parts will be shipped in the industry this year. Sick expects that the industry will face a more orderly transition as it shifts from 64-K to 256-K, compared with the previous move from 16-K to 64-K. For one thing, the economy is better, he says, and cost structures are more equal between U. S. production and Japanese firms. Sick also notes that when the Japanese launched 64-K chips, they were not major competitors in the 16-K dynamic-RAM markets. "They had nothing to lose," he adds.

One source at Mostek Corp., Carrollton, Texas, agrees with Sick's assessment of the marketplace, noting that the 256-K generation is starting out in much the same atmosphere as the 16-K did in 1979–80. The 64-K chips, on the other hand, hit the market when demand was flat. So the 256-K life cycle and pricing patterns may be closer to those of the 16-K generation. Some customers are already locking in commitments on future 256-K chips at premium prices, parallelling the situation with 16-K chips in their early days, when customers were locked into paying $5 to $6 per chip even after prices fell almost overnight below $3.

tions as they come up," believes Perry Constantine, vice president for North American marketing at LSI Logic Corp., Milpitas, Calif. "We're standardizing everyone's custom needs," he points out.

Henri Jarratt, president of VLSI Technology Inc., San Jose, believes the strength of the U. S. economic recovery played a large part in the current boom in application-specific chips. "If the economy had come out of the recession more slowly, all the big semiconductor houses could have supplied parts to equipment vendors," he says. "But we came out quickly, and companies couldn't supply the parts." This situation, he adds, "accelerated the custom business."

Yet shortages of standard parts alone are not enough to justify the boom. Equipment manufacturers "see the need for new advances in technology," Jarratt says—advances that vendors of application-specific ICs think only they can provide. "The custom changeover was coming anyway, but the boom helped advance this," notes Bill Loesch, vice president, strategic planning, Zymos Corp., Sunnyvale.

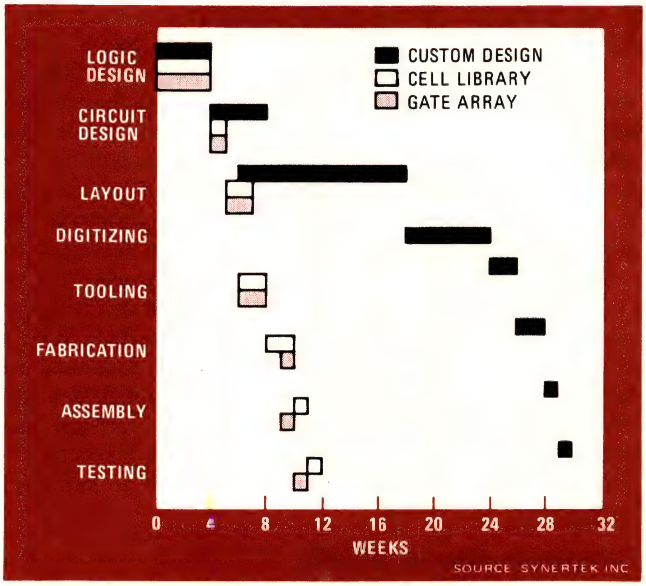
Making application-specific ICs more attractive and easier to deal with is the use of new tools whose development has been hastened by advances in chip technology and which in turn hold the key to future chip advances: CAD work stations. New work stations from such vendors as Daisy Systems Corp. and Valid Logic Systems Inc., both in Sunnyvale, and Mentor Graphics Corp., Portland, Ore., are putting increased power in the hands of circuit designers. Moreover, software development by work-station vendors and application-specific-IC manufacturers is enabling end-user equipment manufacturers to meet their performance requirements more quickly and easily. "The tools that allow a simple engineer to [design circuits] are fast moving into their hands," says Dataquest's Bogert. "Growth in CAD is booming, and it has just scratched the surface."

For now, buyers of application-specific ICs are tied to the particular CAD system and software offered by particular vendors of these chips. They use this hardware and software system either at the vendor's site, through a remote linkup, or at their own sites, through installed equipment. After design engineers are trained on the CAD system, the customer, working to some degree with the vendor's staff, designs a chip.

The design is transmitted to the IC's manufacturer, which produces a prototype of the chip for testing and inspection to make sure it meets the designer's requirements and specifications. If everything is satisfactory, the vendor starts manufacturing chips.

Design tied to manufacturing

LSI Logic's Constantine does not see any way to separate the design function from the manufacturing function for vendors of application-specific ICs and their customers. That, he says, is because the task of designing a chip involves two stages: "designing something that logically works, and making sure it performs with the manufacturer's silicon. To do that, you need software that ties the two together. There is no way a semiconductor manufacturer can be bypassed, either from the software or the silicon standpoint."



5. Time savings. Application-specific integrated circuits, such as cell libraries and gate arrays, require shorter design cycles than full-custom ICs. This is one of the advantages chip manufacturers say that the technology offers equipment designers.

Large standard-semiconductor manufacturers, looking at the potential of the semicustom-IC market, are trying to standardize design and manufacturing procedures so that they, too, can take part in the industry. Creation of an industry-standard interface language for computer-based chip-design tools will speed the market's growth and change some of the ways firm compete, claims H. Wayne Spence, vice president of TI's Customized Components division, in Dallas.

Work on a proposed standard—called the electronic design interchange format—is now being undertaken by a consortium made up of TI, Motorola, National Semiconductor, Tektronix Inc., Daisy Systems, and Mentor Graphics, as well as the University of California at Berkeley [*Electronics*, Jan. 12, 1984, p. 41]. TI was instrumental in starting the effort, and its own Tidal (Transportable Integrated Design Automation Language) system is EDIF's basis

"Anything that you can do to reduce the risk to the consumer in getting his product through—either in design or manufacturing—will cause him to adapt the methodology faster," Spence says. "It [a standard interface language] also makes it more difficult for any vendor to have a CAD niche and use it for a significant advantage in maintaining a customer base."

With an industry-standard interface, customers can take on large projects, with a number of semicustom chip designs, and divide production among a number of manufacturers. Without a standard interface language, design groups would have to use several different CAD systems or spend time converting software.

And with the interface standard, the large jellybean manufacturers can get more heavily involved in the industry that promises such high rewards. "It's almost a given that the market will be large enough for the large companies to get into the custom and semicustom business," observes Bruce R. Bourbon, vice president and

50 Semiconductor Research contracts, with individual pacts ranging from $75,000 to $1.3 million.

Goals for 1990 include integratable high-speed logic elements with state discrimination capability in the 5-to-10-femtojoule range, compatible interconnection of technologies on the same piece of silicon, high-density dynamic RAMs, logic chips with more than a million gate equivalents, accurate 16-bit analog-to-digital and digital-to-analog conversion, and field-reconfigurable ICs.

In the late 1960s and 1970s, "the industry grew so rapidly and the jelly-bean chip manufacturers became so big that Bell Labs and the Government were unable to play the same role," explains Burger. "The role of the university got quite small, and the transfer of technology was so inefficient that U. S. companies ended up duplicating efforts. Redundancy became the characteristic of semiconductor R&D."

Tipping the scales in favor of jointly sponsored R&D was the 1970s entry of aggressive Japanese chip companies and their startling success, says B. R. Inman, president and chairman of Microelectronics & Computer Technology Corp., Austin, Texas (Fig. 6). Starting formal operation in January 1983, the private R&D cooperative has 16 shareholders who have committed millions of dollars to jointly develop new technologies in packaging, software, CAD, and advanced computer system architectures. It is now setting up its own research facilities in central Texas.

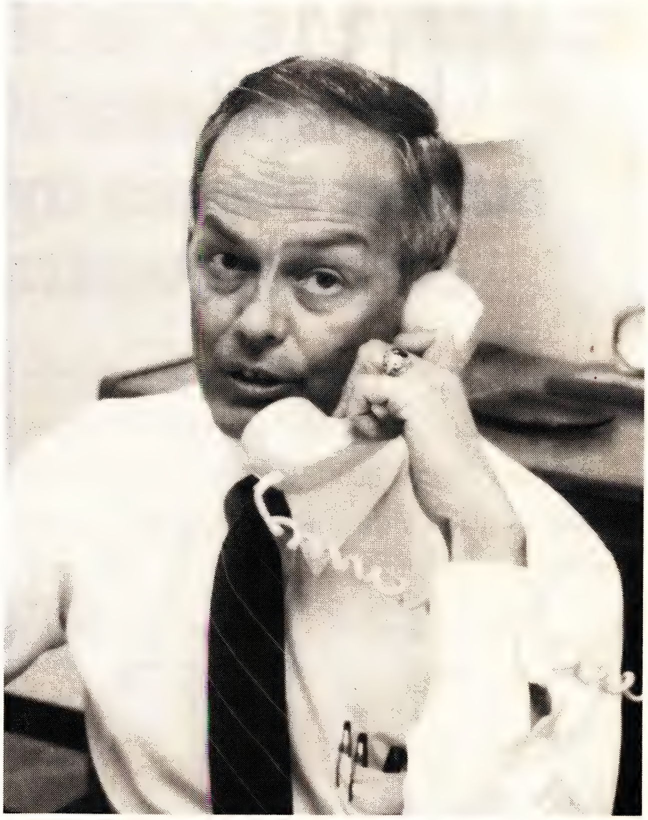
In April, the cooperative announced an associates program designed to encourage the involvement of small firms that cannot afford the cost of a full membership [*Electronics*, April 19, 1984, p. 56]. The program makes available nonproprietary information on developing technology before public release. For its part, Semiconductor Research—which bases fees on prospective members' size—points to its diverse list of members, which represents a cross-section of the industry.

Small firms' spending is limited

"Small firms cannot afford the research beyond their initial products—they have to commit much of their resources on day-to-day survival," Inman states. "Companies that are larger need long-term developments for long-term profitability." In nearly every case, the cooperative's shareholders thought they could not individually afford the price of these long-term projects, says the retired U. S. admiral and former deputy director of the Central Intelligence Agency.

"They are willing to bank on their talents to market and produce while not wanting to be left behind in new technologies," he adds. In addition to combating government-aided competition from abroad, Microelectronics & Computer Technology is aimed at ensuring the prosperity of mid- to small-sized firms against the U. S. conglomerates. "The giants really have the resources [to fund their own research and development] to compete," Inman says, adding that membership of only larger firms could spell antitrust woes for the cooperative.

R&D consortiums have friends in Washington, as their cause in Congress—legislation to clear legal hurdles for joint R&D—has seen little opposition. The House of Representatives has unanimously passed a bill designed to discourage frivolous antitrust suits against joint R&D efforts. The bill eliminates treble damages and requires losing parties to pay the winner's attorney fees.



6. Cooperate. Small firms need to combine their research and development work in order to survive in today's technologically competitive market environment, argues B. R. Inman, chairman and president of the Microelectronics & Computer Technology Corp.

"There seems to be a political will in Congress to pass this type of legislation," says Bill Bartolone, manager of government affairs for the American Electronics Association, in Washington, D. C. "They realize there is a lot of duplication [of R&D] in the American industry, and now the whole worldwide competeviness comes into play."

However, warning of a demise of competition in the electronics industry, Joseph M. Alioto—a San Francisco antitrust attorney—complains, "This is not free enterprise, and it is not American, period." Alioto, who has written a letter of protest to each member of MCC and appeared before hearings in Congress, thinks the legislation will discourage all legal challenges because "small firms and new startups will not risk their entire business to sue these combines—which, due to cost of membership, are made up of big firms.

"I think this is a result of a false hysteria with regard to fear of unstoppable competition from the Japanese, and there is no evidence [of teaming up to dominate U. S. markets]," insists Alioto. Many participants are now hoping to sharpen their competiveness against other U. S. firms by way of joint R&D ventures, he adds.

Contributing to this report were correspondents Kevin Smith, Robert Gallagher, and John Gosch in Europe, and Charles L. Cohen and Mike Berger in Japan. ☐

gated to the array input/output buses and amplified further with a set of secondary sense amplifiers and output buffers to drive the off-chip load capacitance.

The 51C256 memory array is organized as eight blocks with folded-metal bit lines and polysilicon word lines. Dual row decoders and drivers reduce the delay on the polysilicon word line to speed access. A negatively bootstrapped word line allows the full supply-voltage level to be written in the memory cell. Each of the eight memory blocks is further divided into halves by a set of multiplexed primary sense amplifiers. This reduces the bit-line length and improves the bit-line–to–cell-capacitance ratio to provide a respectable 190 millivolts of sensing signal.

Signals are sensed by a clocked p-channel latch that is totally isolated from its bit lines during sensing (Fig. 2). A pair of capacitors attached to the internal sense-amplifier nodes is activated before sensing to perform the functions of trip-point adjustment and gain improvement. The bit lines are actively restored by n-channel-transistor latches on both sides of the sense amplifiers. The bit lines are actively held at the power-supply potential (V_{DD}) or ground (V_{SS}) during the normal precharge time. They are equalized early in the active cycle, thus pipelining a portion of the precharge into the next cycle and decreasing the memory-cycle time.

Signal sensing in the array is done with a half-V_{DD} level on the bit lines to eliminate the need for a dummy cell and to reduce the active-power and peak-supply currents. Half of the bit lines are sensed from half V_{DD} to V_{DD}; the other half are restored from half V_{DD} to V_{SS} during the active cycle. Supply-current peaks are further reduced by staggering the sets of n-channel restore latches in the active and precharge periods. The half-V_{DD} sensing scheme also speeds up the charge transfer from the memory cell to the bit line and enhances the access time.

Redundant rows and columns have been incorporated in the 51C256 in order to improve the manufacturing yield. Random defective-element replacement is accomplished by electrically programming polysilicon fuses that have been selected with a shift register.

TABLE 1: C-H-MOS III-D TECHNOLOGY

Feature	Description
Substrate	p-type epitaxial layer on heavily doped p-type substrate
C-MOS well	3.5-μm-deep n-well
Number of polysilicon layers	2
Minimum feature size/alignment	1.5 μm/0.5 μm
Parallel-plate plasma-etched layers	nitride, polysilicon, oxide, and aluminum
Bird's beak of storage capacitor	$<$0.2 μm
Thickness of cell-storage dielectric	$<$ 150 Å
Transistors	250 Å/1.2 μm with graded n^+ junctions
Junction depth	0.3 μm
Redundancy	electrical polysilicon fuses

The 51C256 has four I/O array buses to provide direct conversion to the four-output configuration. This configuration is attractive for small memory systems requiring higher data bandwidth and lower active power. The peripheral and array-support functions of the part are designed with both static and clocked C-MOS circuits to achieve high speed and wide operating margins. With the dual–row-decoder design and H-MOS III transistor scaling, the 51C256 has a typical row-address-strobe (#OL1#RAS) access time (t_{RAC}) of less than 100 nanoseconds and a typical precharge time (t_{RP}) of less than 50 ns.

The C-H-MOS III-D technology uses two layers of polysilicon and state-of-the-art process modules. A cross section of the memory cell and the MOS transistors in this technology is shown in Fig. 3. A p-type epitaxial layer on a heavily doped p-type substrate is used to reduce the effective substrate resistance. This also en-

2. Isolated. Signals are sensed by a clocked latch that is totally isolated from its bit lines during sensing. All transistors inside the tinted areas are p-channel devices; others, such as the latches that actively restore the bit lines before sensing, are n-channel devices.

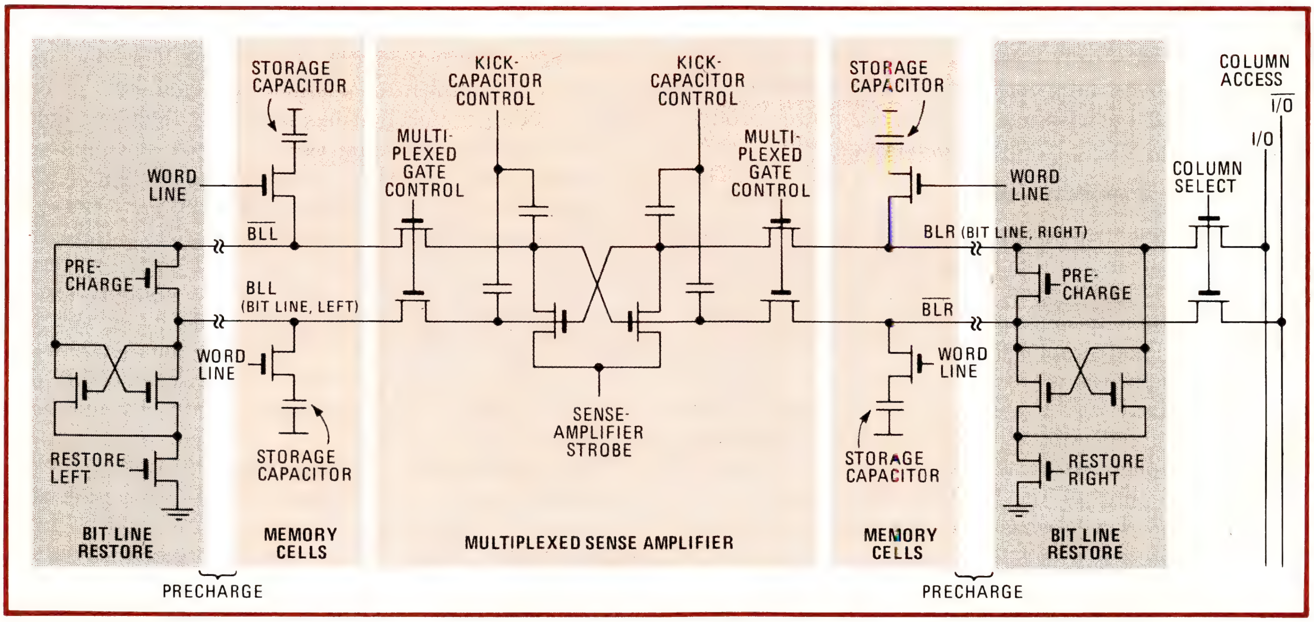


TABLE 2: EVOLUTION OF MOS TECHNOLOGIES

	Enhancement-mode n-MOS	Depletion-mode n-MOS	H-MOS I	H-MOS II	H-MOS III	C-H-MOS III-D
Year of introduction	1972	1974	1977	1980	1983	1984
Channel length (μm)	6	6	3	2.0	1.2	1.2
Gate-oxide thickness (Å)	1,200	1,200	700	400	250	250
Junction depth (μm)	2	2	0.8	0.5	0.3	0.3
Shortest gate delay (ns)	12	4	1	0.4	0.2	0.2
Speed-power product (pJ)	18	4	1	0.5	0.25	0.01

simply a string of inverters arranged to drive a given capacitance load. In C-H-MOS III-D, an inverter delay can be as small as 0.20 ns; the number of inverters and their device sizes are chosen according to the output load for optimum speed.

To reduce the supply-current drain and drive the output load with full supply-voltage levels, the n-MOS generator uses push-pull drivers and internal bootstrapping. This results in an inherent delay associated with the precharge and the release of the internal bootstrap capacitances. The C-MOS driver not only occupies less silicon area but it is also more efficient in driving the output load, thus dissipating less power and running cooler.

The C-MOS clock driver also provides a higher output-current drive per input capacitance. Therefore, smaller inverters may be used with C-MOS circuits at the input stages for TTL-to-MOS-level conversions and then amplified on chip with other inverter stages. This results in lower input capacitance and smaller dc-current drain for an input stage with TTL levels applied.

The architecture of the 51C256 and its C-MOS circuit design result in lower active, standby, and refresh currents than those of its n-MOS counterparts. The active current is typically less than 45 milliamperes at a 240-ns cycle time. The maximum peak supply current is just 130 mA, and the standby current with C-MOS input levels is typically under 5 microamperes. Furthermore, the sum of its refresh and standby currents is less than 230 μA with extended 32-millisecond refresh periods.

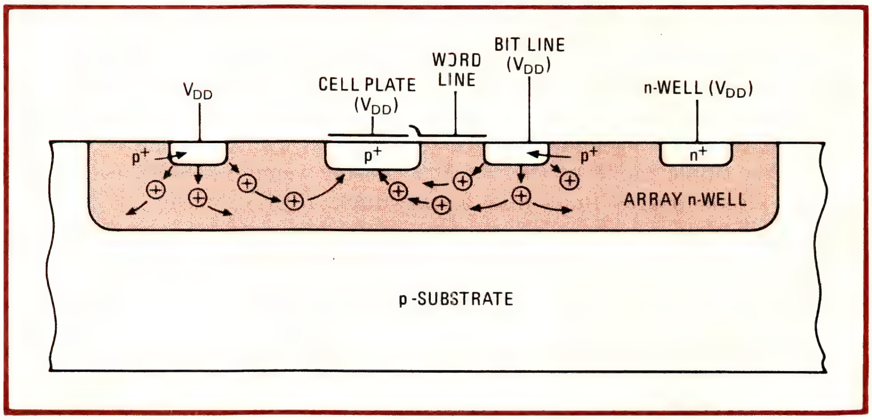
The half-V_{DD} sensing scheme employed in the memory array saves about 10 mA in the active current; in addition, it reduces the supply-current spikes, which are further reduced by staggering the bit-line restore function in the active and precharge periods. The C-MOS clock drivers and input buffers produce a substantial reduction in the power needed to drive the various capacitive loads around the chip.

Also, the use of select-type C-MOS decoders reduces substantially the supply currents in charging and discharging the row and column decoders, which is usually one of the largest current problems in dynamic-RAM designs. In the conventional n-MOS deselect-type decoder, a number of internal nodes are charged to V_{DD} and then as the address lines become valid, all but one of the decoders are discharged and deselected. This results in a significant substrate bounce, which may cause unwanted injection and coupling interferences. With C-MOS circuits, a select-type decoder, in which only the selected decoder is required to move, is possible without a dc-current drain. This also reduces the internal and external current spikes and the substrate-bounce effects. Further dampening of the power-supply current spikes and noise is achieved in the 51C256 with the additional V_{DD}-to-V_{SS} capacitance provided by the memory-array n-well capacitance to the substrate.

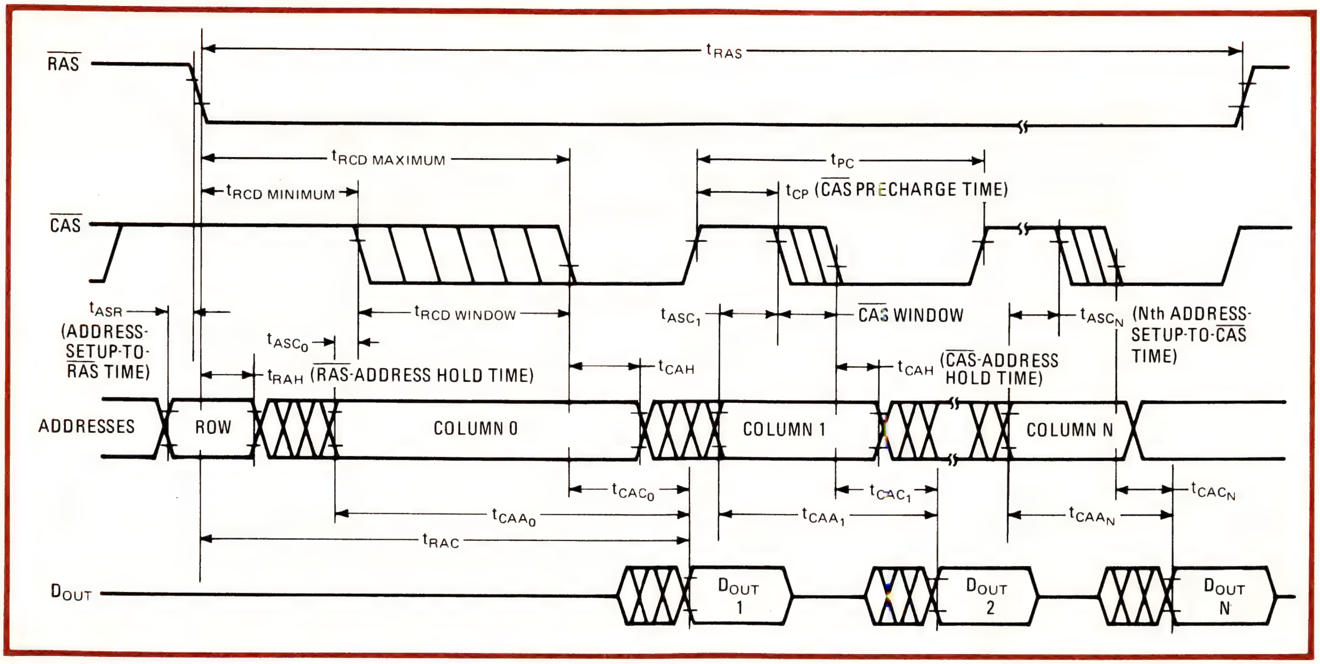
Another factor is that the use of C-MOS circuitry in the input stage of the $\overline{\text{RAS}}$ buffer of the 51C256 results in low standby current limited only by junction leakage. It is typically less than 5 μA with C-MOS input levels, with a maximum specification of 100 μA. Even with TTL inputs, the standby current would increase to only 2 mA. Another attractive feature of the 51C256 is an extended refresh capability of 32 ms.

High-bandwidth data streaming

It is well known that the refresh characteristics of n-MOS dynamic RAMs are usually limited by thermally generated carriers from defect sites in the substrate within a diffusion length of the memory cells. These minority carriers degrade the refresh times. Embedding the memory array in a reverse-biased n-well dramatically reduces this thermal leakage current. The n-well confines the minority carriers to those thermally generated in the n-well, whose depth is substantially less than a diffusion length. The doping gradient of the n-well results in a retarding field that reduces further the collection of these minority carriers.



4. Carrier injection. Coupling from transitions of nodes in an n-well that is not biased above V_{DD} can generate short-duration local forward bias and carrier injection from other nodes held at V_{DD}. All carrier-injection sources must be carefully suppressed.



5. Usable speed. Design at the system level is simplified by the 51C256's static circuits, as seen in the timing scheme for access with multiplexed addresses. The available window for the delay time between $\overline{RAS}$ and $\overline{CAS}$ (t_{RCD}) is much larger than it is in its n-MOS counterparts.

now obtain the dynamic-RAM benefits of lower power and higher density.

The 51C256 is designed to deliver high reliability with high performance. Especially engineered for the part is a new 16-lead, 300-mil-wide, dual in-line plastic package that meets stringent criteria for mechanical stability and moisture immunity. With its low active power and the package's low thermal resistance, the 51C256 runs very cool.

In fact, its operating junction temperature is only 12°C above the case ambient temperature, which is substantially lower than that of its n-MOS counterparts. Most physical phenomena that limit the active life of dielectrics, interconnections, contacts, and transistors are thermally activated and hence are retarded substantially with the lower junction temperature.

The reduced transient and average current densities on the aluminum connections also result in better design margins for electromigration. Special screening tests were designed for the new RAM to efficiently screen the various dielectrics, polysilicon fuses, and high-speed transistors during wafer sorting. Thus, the 51C256 maintains rigorous reliability standards with its aggressive scaling of transistors and dielectrics.

Latchup-free design

The 51C256 also delivers a soft-error rate better than the industry standard of 0.1% per 1,000 hours of device time at a 7-microsecond cycle time for the n-MOS 64-K dynamic RAM. With a 1-μs cycle time and 4.75-volt supply, the soft-error rate is less than 0.1% per 1,000 h. The 51C256 achieves its low soft-error rate without die coating by virtue of its high storage-cell capacitance and its unique architecture. The memory cell, bit lines, and sense amplifiers are all embedded in the n-well, which reflects the carriers generated from alpha-particle tracks in the substrate, as shown in Fig. 3.

The 51C256 is designed to be immune to latchup under all practical operating conditions. As the supply voltage, V_{DD}, is increased up to 16 V, the supply current increases gradually due to nondestructive junction breakdown, but the device does not latch up. Forcing large dc currents and voltages on the input and output pins at 125°C also does not cause the 51C256 to latch up. The excellent latchup immunity of the 51C256 against internal and external noise sources has been achieved with the use of a p-type epitaxial layer on a heavily doped p-type substrate and the application of transient latchup guidelines.

The 51C256 design illustrates how the combination of C-MOS technology and novel architecture can propel dynamic RAMs to new performance levels and applications horizons. C-MOS makes possible new circuit implementations that were not practical with n-MOS. For example, the 51C256 uses clocked latches for the primary-signal-sensing and restore functions; a half-V_{DD}-sensing scheme to achieve lower active power and wide operating margins; and static column decoders, address buffers, and internal data path to provide high usable speed and data bandwidth with ripple and static-column modes. Furthermore, the use of C-MOS circuits in the input $\overline{RAS}$ buffer, along with the elimination of charge-pump circuits, provides microwatt standby power; a p-channel memory array in an n-well improves refresh characteristics, reduces soft errors, and shields the memory cells from spurious carrier injections in the substrate.

The 51C256 can meet the requirements of a variety of applications where previous memory generations failed. These include those needing high data bandwidth and density (graphics, signal processing, and cache memories), low power and high density (portable and remote systems), usable speed, and high reliability—all applications that are projected to be among the fastest-growing segments of the memory market. ☐

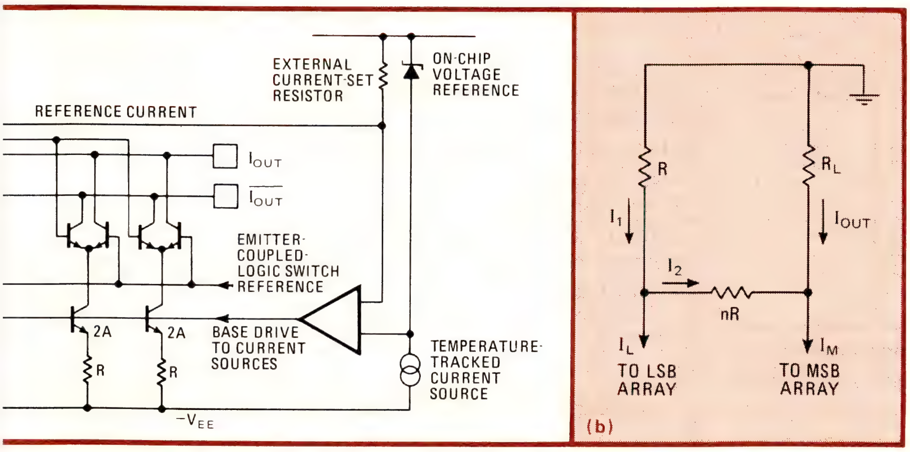
switch currents are at equal current densities (except the 0.5- and 0.25-value sources, but these are nondominant terms). Since the devices operate at very closely matched speeds, the output glitch content is therefore minimized.

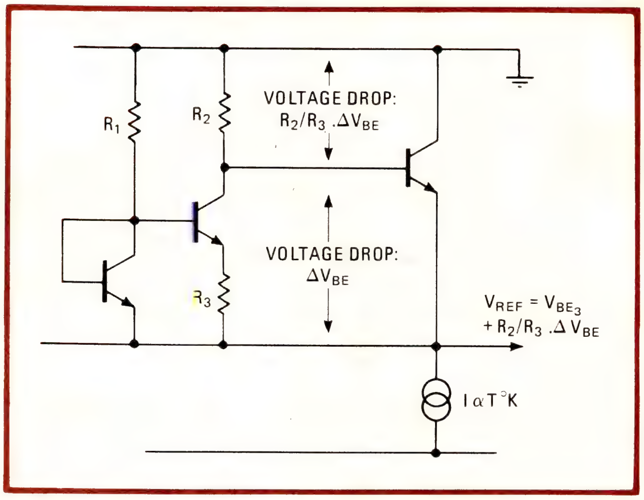
The multiple-current-source array also aids accuracy and thermal tracking performance. Within the array, four current-sensing transistors used in a feedback loop set the output current range by means of the single external current-setting resistor. The current sources are interdigitated in order to spread any potential process and thermal mismatch through the array. The reference loop ensures that the output current depends only on the voltage reference, which is provided on the chip, and on an external current-setting resistor that can be of any specified accuracy and temperature coefficient. In order to achieve an overall variation, with temperature, of less than 50 parts per million per °C, the chip's voltage reference typically has a temperature coefficient of 30 ppm/°C.

Minimizing errors

The chip's layout is equally important in achieving the required accuracy. Potential sources of error are random or systematic variations in resistor and transistor parameters; generally, these variations occur as local gradients across a silicon wafer. Interdigitation of multiple current sources on the 9770B has been used to offset process-induced parameter gradients and possible temperature gradients. All resistors in each array are parallel and identical, with identical voltage drops to avoid field effects and potential nonlinearities.

Because the isothermal layout of multiple current sources cancels the effects of thermal gradients, no change in the output is observed when an arbitrary heat source produces a thermal gradient. In addition, the feedback maintains the average current level, determined only by the voltage reference and the off-chip current-setting resistor. If another orthogonal heat source exists simultaneously, however, it does affect the current sources unequally. But since the four MSBs are spread through the array, the effects of the temperature gradient are averaged out. In practice, this averaging is only an approximation but it is a useful technique, and one that is not available in the traditional d-a converter's R-2R array.


EXTERNAL CURRENT-SET RESISTOR
ON-CHIP VOLTAGE REFERENCE
REFERENCE CURRENT
I_{OUT}
$\overline{I_{OUT}}$
EMITTER-COUPLED-LOGIC SWITCH REFERENCE
2A
2A
BASE DRIVE TO CURRENT SOURCES
R
R
$-V_{EE}$
TEMPERATURE-TRACKED CURRENT SOURCE
R
R_L
I_1
I_{OUT}
I_2
nR
I_L
I_M
TO LSB ARRAY
TO MSB ARRAY
(b)


R_1
R_2
R_3
VOLTAGE DROP: $R_2/R_3 . \Delta V_{BE}$
VOLTAGE DROP: ΔV_{BE}
$V_{REF} = V_{BE_3} + R_2/R_3 . \Delta V_{BE}$
$I \alpha T°K$

2. On-chip reference. The converter's on-chip voltage reference uses only conventional npn transistors and implanted resistors. The configuration is essentially the classical Widlar compensated diode.

The central metal track covers the main resistor array, with resistor widths of 40 micrometers that ensure good matching and relative freedom from effects due to process variation. Current-source transistors, both above and below the resistor array, have dual 4-by-10-μm emitters; half-value sources have only a single emitter, and the quarter-value source has a 4-by-5-μm emitter.

Dummy components at the ends of the resistor array were avoided by ensuring that the end elements hold the least significant bits. Distribution of the negative rail is important in matching, and low voltage drops have been achieved by the use of a wide track across the array. In addition, the converter has bond pads at both ends of the array to reduce voltage drops to the central current sources.

On-chip voltage reference

Most monolithic d-a converters do not have an on-chip voltage reference, primarily because of the difficulty of designing a stable bandgap source that does not exact a penalty in chip area. Designers of earlier d-a converters observed that the use of an on-chip reference was desirable from the end-user viewpoint and that a relatively simple design could satisfy many requirements. The circuit configuration (Fig. 2) is essentially the classical Widlar compensated diode[1], modified to operate with the upper connection grounded. This leads to an adequate reference-temperature stability (around 35 ppm/°C) without recourse to pnp devices or trimming techniques. Where very high-temperature stability is required, an external reference can be provided to the converter reference input.

The reference-loop operational amplifier discussed above is a straightforward all-npn design, similar to that used on an earlier 8-bit converter. Power-supply rejection is 60 decibels, the common-mode rejection ra-

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cols all the way from the physical to the transport layer and is actively developing standards in the upper layers as well.

Mainframe and minicomputer manufacturers played a major role in the initial definition of the mechanisms required in networking. But they have not yet pushed for standardization, because up until now networks have been set up mostly in homogeneous systems environments where the problem of transferring data across equipment from different manufacturers was unimportant or resolvable by slow data-transmission mechanisms. Except for IBM's System Network Architecture, these proprietary networks will probably not have a large market impact outside their captive customer bases.

Although there is almost no direct compatibility among manufacturers' protocol structures, there is some similarity, and it is possible to make a rough alignment with the OSI model (Fig.1). Most of these manufacturers, including IBM, say they intend to provide OSI-compatible protocols for open systems, but how soon and how extensively they will do so is not yet clear. Certainly, their massive investment in proprietary protocols will not be scrapped overnight.

Another big player in the standards world is the International Consultative Committee for Telegraphy and Telephony, the regulating body of the telecommunications world, whose standards reflect its vested interest in the installed base of telecommunications systems. CCITT's tack will resemble the course that major manufacturers have taken with their proprietary networks, but its position carries much weight, and the S-series protocol standards from this organization have become an established part of all attempts to standardize layers.

State of the art

Most parties to the ongoing debate on standardization accept the partitioning of functions outlined in the seven-layer model, so the task of implementing protocols can be broken into more manageable components. A substantial measure of agreement exists on the details of the transport layer and on certain areas of the presentation layer, and as a result it is now possible to connect heterogeneous nodes on a local network and to have them pass data among themselves in a highly reliable manner.

The network layer is being defined, but the work has been hampered by disagreement on how the global network should function. Currently, the most common standard is the X.25 protocol used on public data nets, but this covers only the access sublayer and does not address the problems of harmonization or internetworking.

The session layer remains a battlefield. The ISO's spirit of compromise has produced a cumbersome proposed protocol that is largely unacceptable to U. S. interests as voiced by ANSI. As a result, the regulation of data transfer still is a matter of taste.

At higher levels of the model, the need for standardization increases, but the number of successfully completed documents is relatively small because of the more pressing needs of the lower layers and the degree of host dependence that functions acquire in the higher layers of the OSI model.

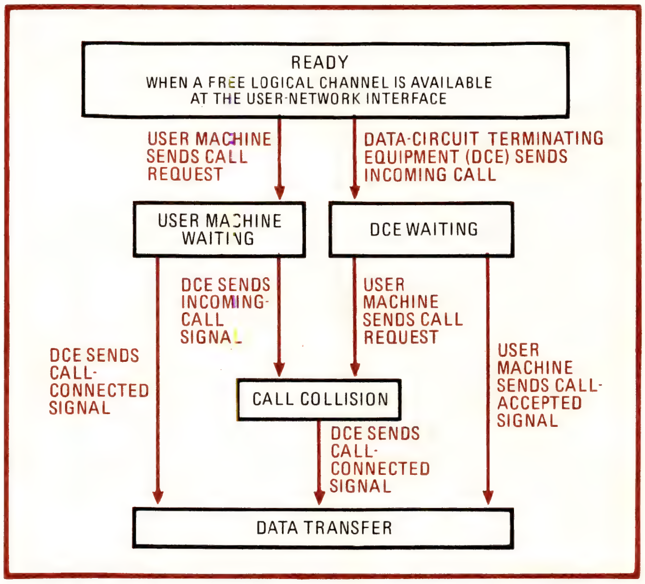
Packet-switched public data networks grew out of Arpanet and use the telephone system as their main network pathway. The protocols, standardized largely by the CCITT, are exemplifed by Canada's Datapac, Britain's EPSS, and the U. S. Telenet.

Packet switching improves the use of transmission paths between computers by permitting a high degree of multiplexing on the lines. Users can therefore vary the data rate to suit the terminal equipment they want to connect. Protocols complement packet switching, since packets provide fixed locations within the transmission, where protocol headers can be located and the frequent administrative messages can be sent.

The most important protocol standard used in switching is the CCITT's X.25, which defines the relationship between the common-carrier packet-switched network and the user machines that employ it. The protocol makes no assumptions about the network's actual construction and is instead oriented towards connections available from common carriers.

The X.25 standard defines the interface between the host, or DTE (data terminal equipment), and the carrier, or DCE (data circuit-terminating equipment). A node that performs packet switching and forwarding functions is called a DSE (data switch exchange). The X.25 standard is concerned only with sending and routing data packets in a network and therefore defines only layers 1 through 3 of the OSI model. It is not concerned with the upper four layers and makes no attempt to define them.

In the X.25 protocol, the network layer is called the packet layer and provides routing and virtual-circuit management, which includes flow control and packet assembly and disassembly. The packet layer therefore includes several functions usually associated with the transport layer in the OSI model. While passing messages across the network, the entity that provides the protocol goes through several logical states (Fig. 2). Any idle virtual-circuit number can be used to designate the connection. The protocol has mechanisms to handle any


READY
WHEN A FREE LOGICAL CHANNEL IS AVAILABLE AT THE USER-NETWORK INTERFACE
USER MACHINE SENDS CALL REQUEST
DATA-CIRCUIT TERMINATING EQUIPMENT (DCE) SENDS INCOMING CALL
USER MACHINE WAITING
DCE WAITING
DCE SENDS INCOMING-CALL SIGNAL
USER MACHINE SENDS CALL REQUEST
DCE SENDS CALL-CONNECTED SIGNAL
CALL COLLISION
USER MACHINE SENDS CALL-ACCEPTED SIGNAL
DCE SENDS CALL-CONNECTED SIGNAL
DATA TRANSFER

2. Packet states. Packet switching across wide-area networks is a reliable way of interfacing heterogeneous networks. During the transfer operation, the protocol evolves though several logical states.

relatively soon, a trend that will reverse itself as the market becomes dominated by standard networks. Because this market is fragmented, specialized systems will continue to provide solutions to the gateway problem.

The major difficulty in connecting wide- and local-area networks is in the difference in the types of network layers involved. LANs will probably use the connectionless protocol; wide-area networks, the more extensive connection-oriented network layer. One of the major requirements is to harmonize network sublayer 3b, where the two different kinds of services meet, so that the internet sublayer can route data between the two. Gateways will also be required for both connection-to-connection and connectionless-to-connectionless types of service, but this presents less of a problem and is not likely to occur as often.

Alternative gateway schemes, where the connection is made at such layers as transport, have been proposed, too. Connections at higher layers make it possible to mask the major incompatibilities of the connection and connectionless types of service networks. At lower layers, the degree of compatibility must be higher, but the gateway becomes correspondingly easier to implement. Figure 3 shows examples of several possible gateway schemes.

The future

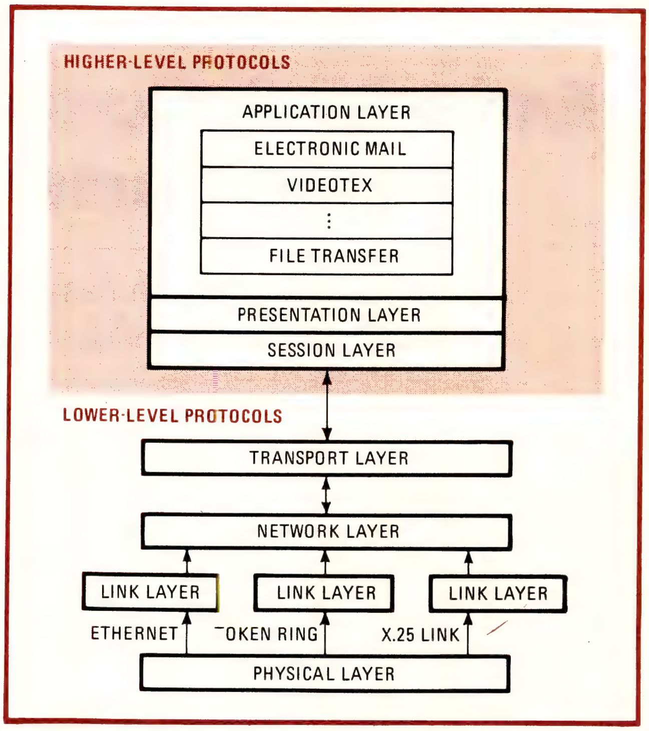
Above all else, the future network market will be characterized by diversity. Just as computers have become ubiquitous in everyday life, so too networks will become dispersed, pervasive, and focused on specific solutions. This is not to imply that they will be incompatible with the OSI model, but the division between the transport mechanism (layer 4 and below) and the transport user (layer 5 and above) will continue to mark different flavors of networks.

Network nodes will be connected through their transport mechanisms. A majority of the functions of layers 4 and below will be standard features of most nodes. Incompatible network technologies will create connections by using gateways. In descending order of importance, the major kinds of networks that will probably be available within five years are likely to be:

- Ethernet and compatible derivatives.
- The IBM token ring and clones.
- The token bus in industrial-control applications.
- Networks based on private automated branch exchanges, with the beginnings of an integrated services digital network.
- Packet-switching wide-area networks.
- Specialized miniature local nets interconnecting microcomputers.
- Proprietary mainframe nets.

The service provided at the boundary between layers 4 and 5 will probably become a universal standard. When this happens, the focus on network technology will fade and the focus on the applications run on the net will dominate.

In layers 5 and above, the protocols implemented in each node are likely to be application-specific—except for mainframes connected to the network, for they will be powerful enough to implement the complete range of protocols. But with the proliferation of intelligent terminals, work stations and distributed data bases, the proportion of mainframe nodes will likely be quite small and decrease with time.



4. Upward to applications. As lower-level protocols mature, it will become easier to implement application protocols, which will probably proliferate as rapidly as application programs do now.

Application-specific nodes will run high-level user protocols that implement subsets of the full set of functions in the top three layers. The major subsets are likely to be videotex in home terminals; encryption in banking terminals; file transfer and distributed-data-base protocols in distributed systems; and electronic mail, videotex, and file transfer in desktop computers.

An indication of the diversity of the application protocols expected in the future is shown in Fig. 4, along with an indication of the major networks on which they will run. As a result of the market's size and potential, very large-scale integration will probably provide solutions for all major network technologies, particularly if none is dominant.

In the higher layers, the standardization that is expected to win out thanks to the widespread acceptance of the ISO's transport-protocol standard will ensure that an integrated solution is available. Higher than this, the degree of agreement drops alarmingly, and there is little likelihood that layers will be defined as clearly as the transport layer is. Since these functions are heavily oriented to software and the node operating system, additional lack of standardization here makes comprehensive hardware solutions unlikely.

What can be expected are a number of support devices that are to the node what floating-point chips are to a microprocessor Likely candidates are the encryption, data-base-access, virtual-terminal, and file-transfer protocols. ☐

less advanced design. Functionality can be added to the instrument at the cost of ROM space only. ROMs are more space- and cost-efficient than most hardware. As prices continue to drop, programmable ROMs and erasable PROMs will be used instead of standard ROMs.

The microprocessor simplifies the instrument's internal wiring because a simple bus can link the controls, the processor, and the controlled hardware. Since the microprocessor can set interrelationships among the instrument's various parts, one piece of hardware can be used for multiple functions without the need for complicated switching. Troubleshooting and other specialized modes are simple to configure, often with no need for extra hardware. Adding sensing hardware and sophisticated control software can create a closed-loop control system for improved performance.

Scheduling tasks

An embedded processor must serve several users, either inanimate or human. In each case, expectations of and interactions with the system differ. Although all interactions can be classified as real-time, interactions with controlled hardware are generally more time-critical than those with a human operator.

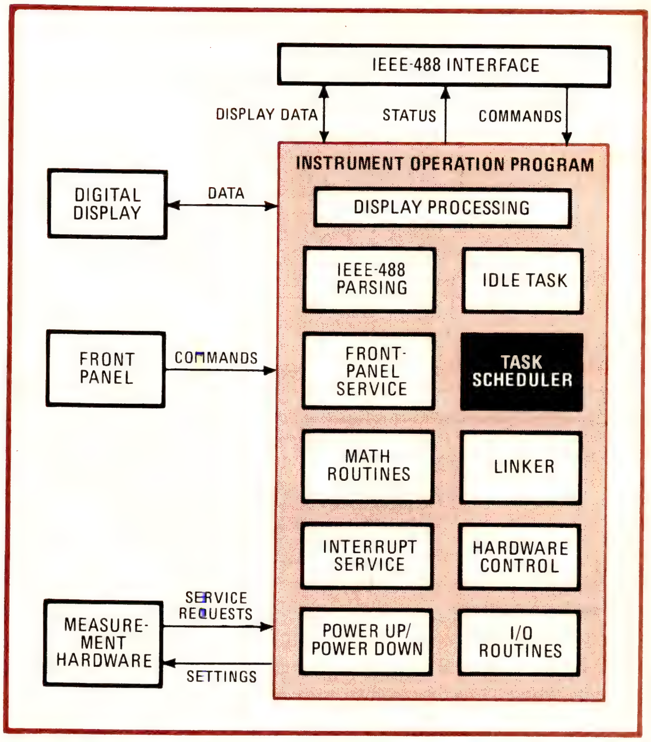
Conventional time-slice multitasking operating systems may not be the best choice for a system with tasks of differing lengths. In addition, although multiple tasks may involve the same hardware, each task might not tolerate any change in control settings until it has been completed.

A self-switching task scheduler is a workable alternative to the time-slice system. In this approach, one firmware task or more handles each control area. While each task can perform a complete and separate function (see Fig. 2), the tasks share common subroutines and can contend for access to the hardware.

Each task is written as an endless loop that must suspend, or transfer, control to the scheduler at least once in each pass through the loop. Suspension usually occurs when the task must wait for a hardware resource or when it has finished its current work. Because the suspending task is in control, it can suspend when the actions of other tasks will not interfere with it and can also prohibit certain actions by using flags. Suspending tasks when they must wait, rather than at arbitrary times, increases system throughput.

To suspend, a task passes a flag's address to the scheduler. The suspending task is not called again until the flag, which may be different at each suspension, becomes set or true. Each time the scheduler is called, it goes to the beginning of the flag-storage table and examines the flag for each task. The first (highest-priority) routine with a set flag is restored to the state from which it was suspended. In the 494 and 494P, the processor's software-interrupt and return-from-interrupt instructions implement the suspend-restore sequence. The scheduler switches tasks by switching stack areas in memory. If no other task has a true flag, the lowest-priority task keeps the processor idle until a hardware interrupt occurs.

With this system, the designer must carefully set tasks by considering the time each takes in relation to how often it is called. Otherwise, two or more high-priority tasks could swap control back and forth, never allowing lower-priority tasks to run. Tasks are called by task-enable flags set either by other tasks or by interrupts. The interrupt-service routines, which exist outside the task structure, only schedule tasks and do not affect the instrument directly.

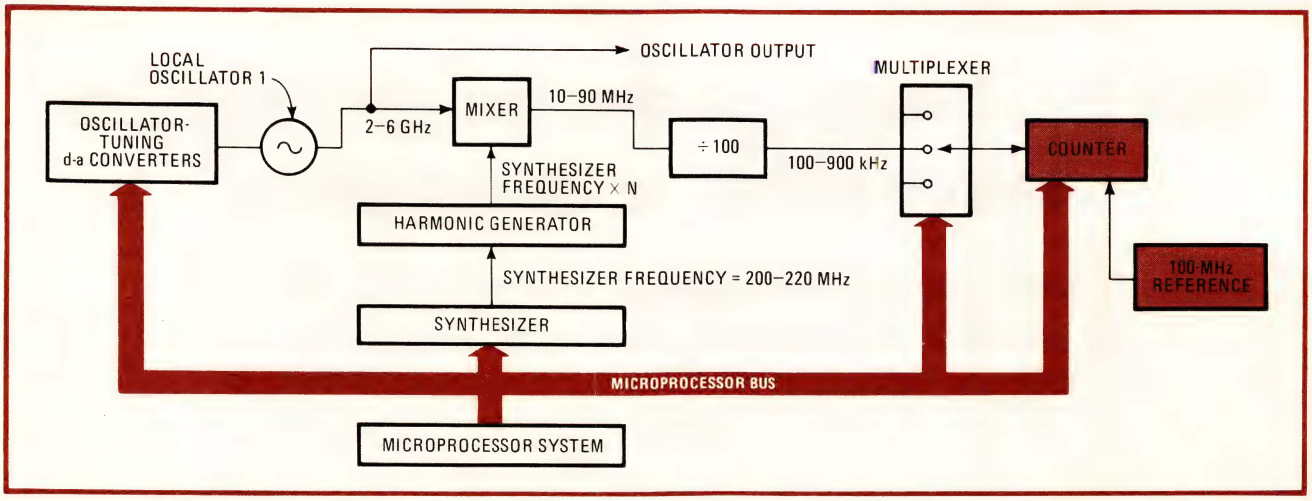


2. A lot to do. The 494/494P's firmware may be roughly divided according to the interface, user, or hardware it serves. Tasks in each area run only when they have something to do. The task scheduler resolves any contention according to a preset priority list.

Embedded systems need to be flexible. Firmware in E-PROM is less flexible than software on disk. For manufacturing and software maintenance, it may be best to support different options, or even different instruments, with the same code. The 494 and 494P configure their firmware at run time. The microprocessor polls the hardware at power-up to see which options are installed, then builds a RAM table with the appropriate routine addresses. Thus a call to the same routine may access different code in different instruments.

No special language exists for programming embedded systems. A high-level language is helpful in structuring the code so that it can be modified and extended. Further, the ability to easily incorporate assembly language can be useful for controlling special-purpose hardware and coding the inevitable time-critical routines.

The accuracy of frequency control determines the analyzer's basic frequency-measurement accuracy. For improved performance, the traditional method of increasing accuracy has been to replace each oscillator with a frequency synthesizer such as shown in Fig. 3a. A firmware-based loop requiring considerably fewer parts than a frequency synthesizer is shown in Fig. 3b. The microprocessor reads the oscillator frequency, compares it to the required value, and controls the oscillator tuning voltage to set the proper frequency. A substantial perfor-



4. First local-oscillator loop. Indirect counting complicates the closed-loop arrangement, but the ratio of complexity to performance is still better than with a direct-synthesizer approach. The 100-MHz oscillator sets counter accuracy and acts as the loop reference.

system but significant in a closed-loop system. The processor finds the signal peak in a filter-response display of the system's 100-MHz calibrator and moves the oscillator until the peak is located at center screen. Counting the i-f signal with the signal counter gives the exact filter frequency. The process repeats for each of the six filters. The filter frequencies are stored in a nonvolatile battery-backed RAM, which maintains the latest value while power is off.

Making life simple

Because the processor can stimulate the hardware and measure the response, it can deduce the hardware's characteristics and determine whether adjustment is needed. One set of routines allows the operator to adjust the tuning d-a converters and oscillator drivers for proper oscillator sensitivity, either during initial factory calibration or after repair. Previous analyzers required external test equipment (signal generators, counters, or both) to make these adjustments. The routines measure the system's sensitivity, display the errors, and guide the operator through the adjustments.

Diagnosing problems in any feedback loop can be difficult, particularly when part of the loop is in firmware, part in hardware, and the loop is active at infrequent intervals. Service functions that open the loop and continuously activate the hardware simplify troubleshooting on the 494 and 494P.

To make sophisticated instruments easy to operate, the designer must tailor the software and hardware so that user tasks can be done as quickly and easily as possible with minimum training. For instance, a spectrum analyzer is a potentially complicated instrument. The center frequency, frequency span, and final i-f bandwidth must be set according to the signal being measured. In addition, to obtain a calibrated display, the span, bandwidth, and sweep speed must be set properly. Also, users must set input attenuation and signal gain according to whether they desire maximum sensitivity or minimum distortion in operation.

The microprocessor aids the user in at least three ways: by providing instrument settings that serve the most common measurement needs, by making it easy to set up the instrument, and by helping the user to cope with unfamiliar controls and procedures. For a given span, the microprocessor can choose the sweep speed and i-f bandwidth to maintain a calibrated display. Before the advent of digital control, automatic selection was usually limited to sweep speed and implemented with analog logic. Today's instruments, including the 494 and 494P, offer both automatic bandwidth and sweep. Thus for most measurements, the operator is concerned only with three controls: center frequency, span, and reference (or input) level.

When a known signal is to be measured, it is convenient to enter settings directly. Each of the three main functions, plus the vertical-scale factor, can be entered using a keypad. During keypad entry, operator prompts on the CRT give brief instructions, the present value of the item being changed, and the allowable range of entries. As another aid, only those buttons that may be used for the entry are lit.

Many advances in user-interface design have been made possible by the recent and continuing increase in memory density. Prompting messages require an amount of text storage that, until recently, would have been impractical in a dedicated system without mass storage. Current E-PROMs, however, have sufficient memory to include a front-panel description in the 494 and 494P in English and in an alternate language.

In addition, modern memory technology allows nonvolatile storage of instrument settings and waveforms. The battery-backed RAM that holds the i-f filter's frequencies and other calibration settings also contains sufficient memory for 10 front-panel setups and 9 waveform displays. For the operator's convenience, the front-panel settings are automatically stored when the instrument is turned off or loses power.

The storage capability is a great advantage for field work, particularly in uncomfortable locations. The necessary measurement settings can be determined and stored in the comfort of an office or laboratory. In the field, the measurements can be made quickly and the results stored for later analysis. ☐

a level 3 system. Its basic hardware layout consists of a standard 19-inch Q-bus backplane, a servo control subsystem, a trajectory–human-interface subsystem, and a power-distribution system (Fig. 1). The main hardware differences between VAL-I and VAL-II lie in their microprocessor boards, main memories, and serial ports. VAL-II has 64-K bytes of complementary-MOS user memory with battery backup, about twice as much as VAL-I. Another 64-K bytes of C-MOS memory contains the operating system. VAL-II also includes a double-sided/double-density disk unit that stores about 10,000 program steps per diskette, or about 1 megabyte of memory. The number of serial ports available to users has been raised from three, for VAL-I, to eight, for VAL-II.

The VAL-II operating system uses a time-sliced control scheme. During operation, about half of each major clock cycle is devoted to arm-trajectory planning and computation. The remaining part is divided up into time slots for the CRT interface, the supervisory computer interface, external path modification, monitor-command execution, main-program step execution, and process-control-program step execution. To ensure that the system can respond to time-critical events as quickly as possible, each task is scheduled to run for a certain amount of time during each major clock cycle. Any event will be received and acted upon within 28 milliseconds of occurrance.

The VAL-II programming language supports all language features available with VAL-I and offers powerful new ones, too—such as user-program I/O and extensive mathematical capabilities, including arrays—for operators of Unimate and Puma robots. VAL-I's features are supported, so users who are adept with that system can develop simple programs on a VAL-II with very little training. For the best use of the sophisticated VAL-II features, experienced users should write the programs. Afterwards, less sophisticated users can maintain them and make minor modifications as needed.

Path modification

Using a RS-232-C interface, the VAL-II system provides a standard path-modification interface called Alter. Robot paths can be modified in either of two modes: world or tool (Fig. 2). The world-coordinate mode refers to the fixed X, Y, and Z directions predefined for each robot; its tool-coordinate counterpart refers to the direction in which a robot is pointing at any given moment. To modify robot motion in real time, users connect an external device to the hardware port of Alter, which every 28 ms transmits data consisting of Cartesian positional offsets in the X, Y, and Z directions and rotational changes about the three axes. Users can specify many different types of modes for Alter. The two most important determine whether the modification will be made in the world or the tool coordinates and whether all the modified data or only the result of the accumulated data should be altered.

Alter makes it easier to interface smart sensors to VAL-II robots. Smart sensors gather data, evaluate it, and then use this evaluation to output information to the VAL-II system. For example, a vision system can correct the position of a robot by using data received from its fields of view. If the vision system notices that the robot's taught path does not correspond exactly to the profile of the current working piece, the VAL-II system can be instructed to correct its motion so that the robot's path follows the piece correctly.

VAL-II can be interfaced to a supervisory computer system through the Digital Data Communications Message Protocol (DDCMP), used by Digital Equipment

Controlling robots with the VAL system

In typical factory environments, different robots work side by side, performing such heavy jobs as arc welding and such light ones as small-parts assembly. Both shop supervisors and programmers stand to benefit from using the same type of control system and robot language for all the robots on an assembly line.

The chief function of flexible control systems like VAL-I and -II from Unimation is getting robots to move and thereby perform specific functions. Two main kinds of arm movement must be specified: first, either straight-line or joint-interpolated motion; second, either continuous-path or point-to-point motion. Continuous-path motions allow operators to specify complex robot paths without stopping the arm. Point-to-point motion can be used when the arm must stop to perform a task.

VAL-I supports three peripheral devices: a keyboard and cathode-ray-tube unit used mainly for robot programming, a teaching pendant that lets operators move the arm when it is in the teach state, and a floppy-disk unit. The control system also gives operators monitor commands that help them start and stop program execution, get robot status information, and single-step through programs. Operators can also specify joint- or straight-line motions.

The system's robot arms are either anthropomorphic (human-like) or polar (circular axis). Joint-interpolated moves require fewer calculations than straight-line motion does, because VAL-II interpolates between the initial and the final position of each joint. Tool-tip motion is hard to predict, however, so joint-interpolated motion must be avoided when obstacles are near or when an accurate path must be followed.

Continuous-path moves can be broken should VAL-I lack enough compute time to calculate the next move's motion time. (About 25 milliseconds are needed to compute motion time.) VAL-II calculates straight-line trajectory commands every 28 ms. Taught points can be stored in either of two ways: operators can define a precision point, which stores the current angle of each robot joint, or they can store the point as a transformation containing the current X, Y, Z, altitude, orientation, and twist information. The transformation values are stored relative to a tool transformation. If an operator has not defined a tool transformation, the end of the joint furthest from the robot base is considered to be the tool tip.

contains no arm-motion instructions—can be run in a VAL-II system concurrently with a motion-control program. Typically, the process-control task monitors and controls external processes by using external binary and analog signal lines. Since the process-control task and the robot program run concurrently, users can monitor many signals while a long robot motion is being performed by the main program. The process-control task can also be used to modify the robot path in real time by using Alter. This path modification can be calculated within the VAL-II system or can be based on various external inputs. (See Table 1 for a sample program.)

Structured constructs

One important feature of the VAL-II language is the way it supports structured constructs, including Case and If-Then-Else statements, While, Do Until, and For loops—valuable programming tools for complex robot programs. For all these constructs, the system automatically generates indented decision levels whenever program steps are displayed on the CRT (Table 2). With constructs, users can organize their programs logically, so code is easier to read and change. These constructs give the VAL-II programming language a degree of power that is similar to systems that are programmed in Pascal or PL/1.

Another important feature of VAL-II is its procedural motion capability, which allows users to define robot motion with mathematical formulas. The VAL-II system can calculate—in real time—the robot motions needed to follow the curve that a formula describes. With a DEC-supplied AXV11-C hardware module, analog I/O functions support specialized VAL-II function and program instructions. The board can handle as many as 16 analog inputs and 2 analog outputs. Using a VAL-II monitor command or program instruction, signals can be sent to any nonstandard I/O address, and input can be received from any nonstandard address.

VAL-II uses real variables in floating-point format rather than VAL-I's less useful scaled integer values. Its other mathematical enhancements include the ability to square a number, to take the square root of a number, and to perform many trigonometric operations. As used here, "number" can mean an expression with multiple arithmetic operators.

The addition of one-dimensional arrays—a feature supported for real variables and location data—shows how the VAL-II language has been tailored for users who have worked with high-level computer languages. By using arrays, moves to locations can be performed in a loop, with the index changing, instead of generating a different Move instruction for each location. Users also gain easy access to a table of real values. Although only 1-d arrays are supported, an array's index can easily be constructed to simulate two dimensions.

When users debug their programs, VAL-II lets programs execute even if the arm power has not actually been turned on. All motion will be bypassed as the program executes, but any errors in its flow can still be found. Another new debugging feature is the way that every program step can be displayed on screen as it is being executed, helping the user find the correct program flow and visualize how instructions are really executed. None of these features is in the VAL-I system.

TABLE 2: STRUCTURED VAL-II PROGRAM

```
. PROGRAM robot
 ; Program to execute one piece of code for odd-numbered
 ;    rows, and a different section of code for
 ;    even-numbered rows until all rows are done.
        10  row = 1 ; Start at row #1
          DO
            IF row MOD 2==0 THEN ; Check for an even row
 ; ODD row
              FOR part = 1 TO col . odd . end
                MOVE odd [row * col . odd . end + part]
              END
            ELSE
 ; EVEN row
              FOR part = 1 TO col . even . end
                MOVE even [row * col . even . end + part]
              END
            END
          UNTIL row == row . end + 1
. END
```

With VAL-II, complex programs can be written much more quickly than they can with level 1 or 2 control systems. Users can up- and and download programs from a central computer with VAL-II. They get increased storage capacity for their programs and can perform functions in the robot while a robot program is running. Finally, programs written in the VAL-II programming language can be understood and maintained more easily than they could be had they been written with level 1 or 2 control systems.

Coming up

To allow robots to track taught points on multiple conveyor lines, an interface with them will eventually be added to VAL-II. Another future enhancement—the ability to pass parameters to subroutines—will let users work with languages more familiar to them. Likewise, they will be able to specify variables and point data as local within a program. All the variables and points will be global by default, which means that all user programs are able to access all global variables. These subroutine features will make it easy to develop easy-to-use VAL-II subroutine libraries

Another future VAL-II enhancement will be the ability to interface and move robots in tandem with welding positioners and gantry systems. Welding positioners, which hold a piece the robot is welding, are used when its range does not extend far enough to reach the whole area to be welded.

While the robot arm is welding one section of the piece, the VAL-II system will instruct the positioner to move it so that the next section to be welded is within range of the robot arm. A gantry system is similar, except that the piece to be welded is stationary and the robot is mounted on a movable gantry. When the section of the piece to be welded comes near the limit of the robot arm's reach, the VAL-II system moves the gantry so welding can continue without interruption. ☐

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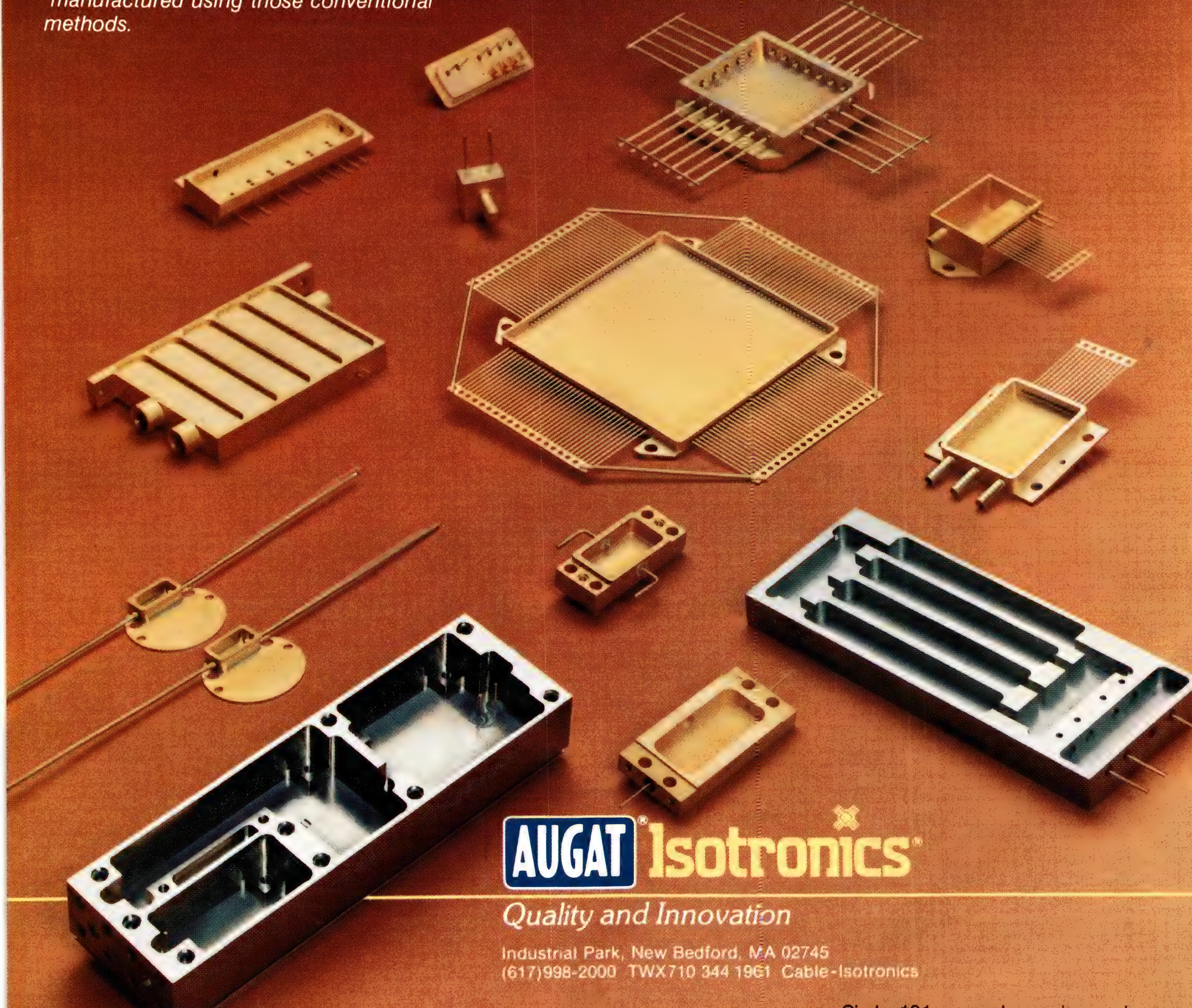

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You need a technological partner with that rare combination of advanced mainstream technologies, a broad line of industry-standard and specialized devices, full-scale production capability, and a proven record of quality and reliability.

RCA has been changing to improve our performance in these critical areas. These changes have been so rapid and so all-encompassing that the only way we can sum them up is to coin a new word: Megachange.

Megachange means that RCA has dedicated tremendous resources to areas that will be the keys to the future, particularly CMOS ICs and power MOSFETs. We're rapidly expanding our already broad line, focusing increased R&D on advanced technologies, and improving already high standards for quality, reliability and customer service.

Megasupplier. Many people think that RCA Solid State's primary business is supplying components to other RCA divisions. Let's set the record straight: more than 90% of our sales are non-RCA.

Our business is supplying active components to companies like yours. RCA Solid State, backed by the resources of a $9 billion corporation, has made the commitment to meet your needs...now and in the future.

We're adding to our already broad line of linear ICs, CMOS logic ICs and power MOSFETs.

We've also begun an active program of alternate-source agreements with companies like Motorola, Philips and LSI Logic.

Megaresearch. RCA has significantly stepped up R&D. The combined expertise of our Princeton Lab, Solid State Tech Center and in-house engineering staff has produced a dramatic increase in new product introductions: 66 in 1981, 171 in 1982 and 295 in 1983.

Our world-renowned David Sarnoff Research Center is a proven source of major innovation, such as the invention of CMOS, the first commercial silicon power transistors, first CMOS μP and first BiMOS op amp. Now we've invented COMFET and logic level MOSFETs.

And we're working on 1.25 micron and submicron geometries.

Megaquality. RCA achievements in quality and reliability have been impressive: an order of magnitude improvement in AOQ over the past four years. And a 95% reduction in failure rate, making RCA reliability excellent.

In many cases, we're setting new standards. For example, our power MOSFETs have a quality level of only 100ppm.

We've also expanded our position as a world-leader in High-Rel power devices and ICs.

Megaservice. We're significantly expanding our force of technically-trained field representatives and field applications engineers. Semicustom design centers are being opened around the world. And we're increasing distributor support with a new on-line order-entry and inventory system to assure you of fast, reliable delivery.

Our distributors and sales reps are a source of pride to RCA. Put their knowledge and experience to work for you and you'll see what we mean.

But the best proof of our ability to be your long-term partner is our track record with customers, including major computer, telecommunication, automotive, industrial and military companies. In many cases RCA is the sole source for a number of critical components.

RCA just might be the right technological partner for you. Call your local RCA sales office. **Or call toll-free (800) 526-2177.**

Photography by Ryszard Horowitz, N.Y.

Changing to serve you better.

RCA

Unit ties together the VLSI design pieces

80286-based engineering work station can handle virtually all steps from design to mask set under the auspices of a single data-base manager

by Clifford Barney, San Francisco regional bureau manager

Only a few years after their exciting but limited beginnings as logic-design tools, engineering work stations are incorporating almost all the functions required for the complete design and layout of very large-scale integrated circuits. The latest offering from Daisy Systems Corp., Sunnyvale, Calif., takes the process from concept well toward mask generation on a single station.

Daisy's Chipmaster maintains a single data base for logical, electrical, and physical layout, and also includes a graphics accelerator that permits the designer to redraw the screen at any level of complexity in real time. The Chipmaster is one of the first systems on the market to be based on the 80286 microprocessor, which is the multitasking, memory-managed member of the Intel Corp. 8086 family.

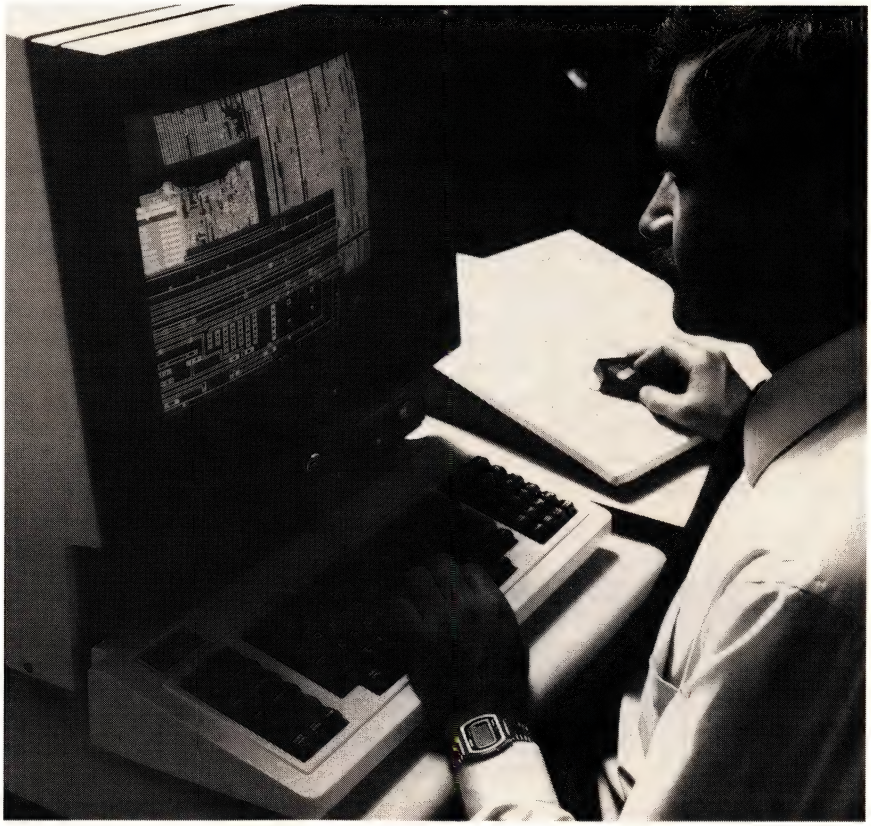
The 80286, which can address 16 megabytes of memory directly and provides 1 gigabyte of virtual-address space, gives the Chipmaster the ability to store information on circuits having millions of transistors. Daisy sees a large instant market in captive and merchant semiconductor houses, whose designers may be performing electronic design by hand and using computers only for schematics and verification, according to marketing vice president John Claiborne.

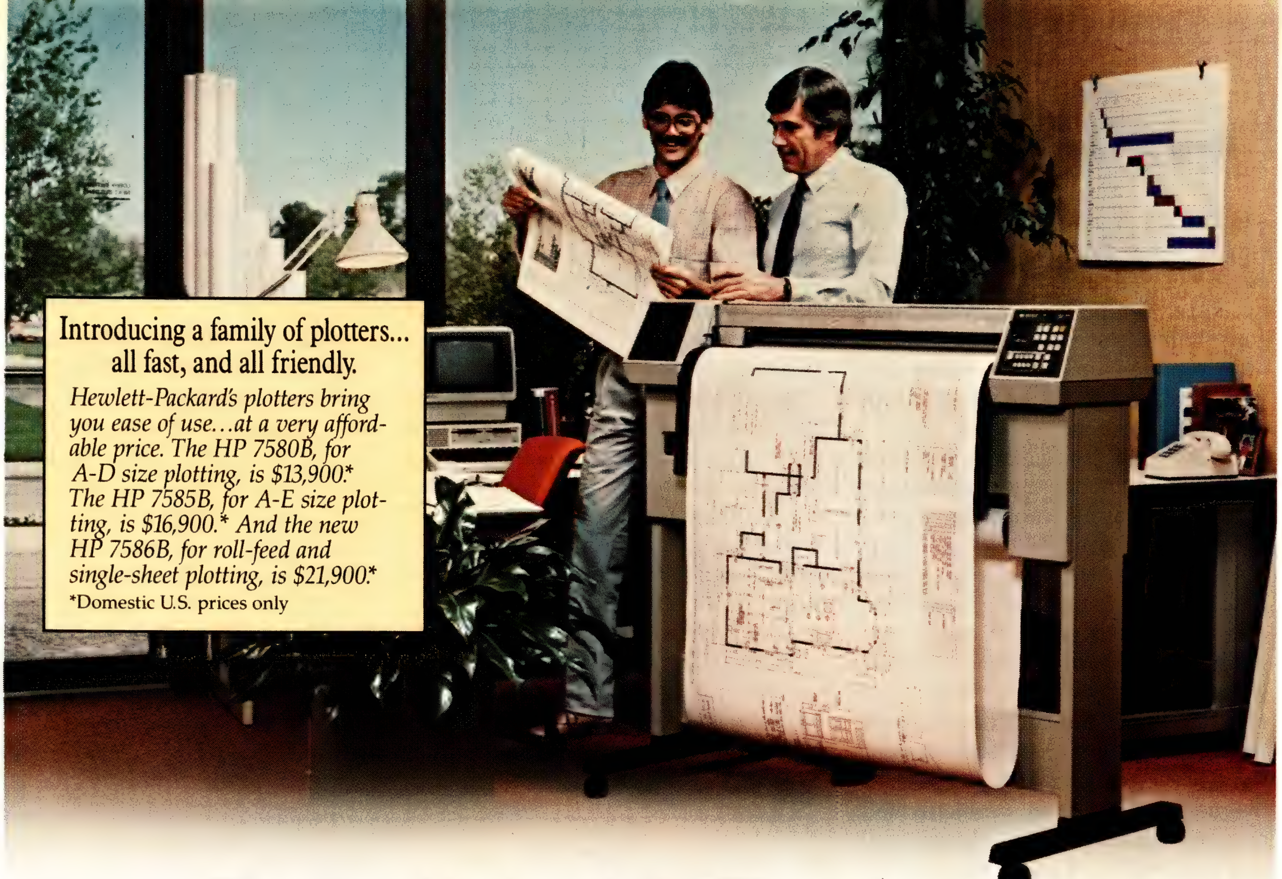
To perform chip layout, Daisy provides a polygon editor called Max, the first of a series of layout tools. Max provides all-angle geometry and can address more than 4 billion points on both X and Y axes. Daisy says that its powerful, hierarchical command structure and hardware support for replicated structures give it twice the performance of larger computer-aided drafting machines for redrawing an edited chip. There is no limit to chip size or complexity.

Max will accompany first deliveries of the Chipmaster. Future tools include chip-planning aids, placement and routing tools, and a hardware compiler that will generate programmable-read-only-memory patterns from a logic-flow chart. Each tool creates its own data base; a data-base manager maps all the information into a single mask-design data base that provides an output to the manufacturing phase.

The data-base manager ensures that design rules are followed during the design process, with no postprocess checking required. It checks connectivity to a point B in drawing a line from point A to point C. It also maps design changes between electrical and physical representations.

Fast graphics. The graphics accelerator, a three-board set built around Advanced Micro Devices' bipolar 29116 bit-slice microprocessor, writes data directly from the data base to the screen, with no conversion to a display file, at a rate of 60 million picture elements/s. A complete chip the size of today's most





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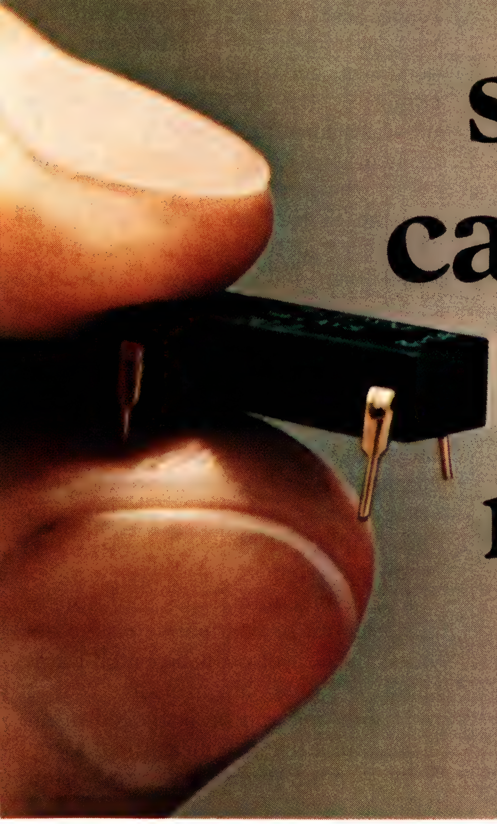

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For complete technical information on the C46F and C47F, call or write. You'll see how and why it makes perfect sense to finally replace all those reed relays for the very last time.

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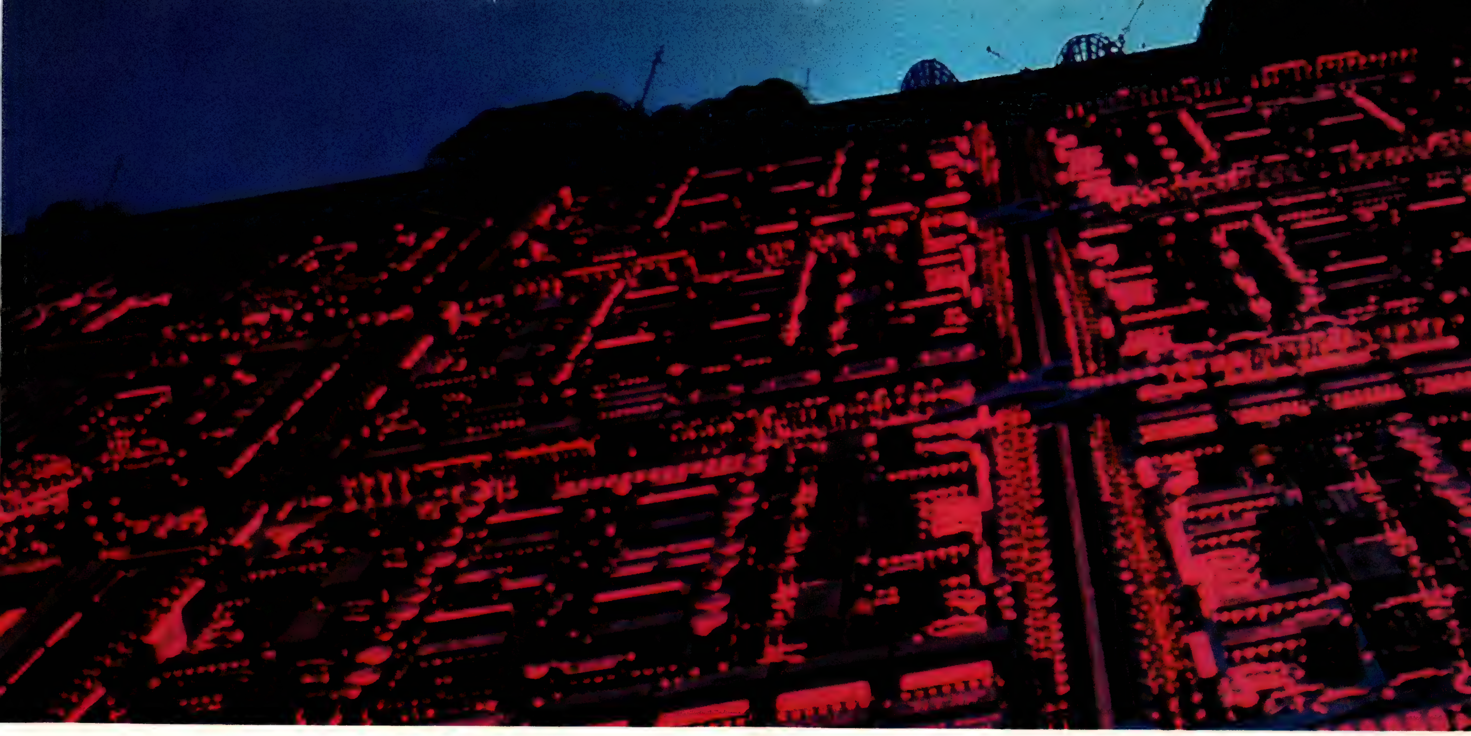

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Testing random logic VLSI chips and memory and linear IC's? The name of the game is throughput. And that's just where Ando can help you roll up the score.

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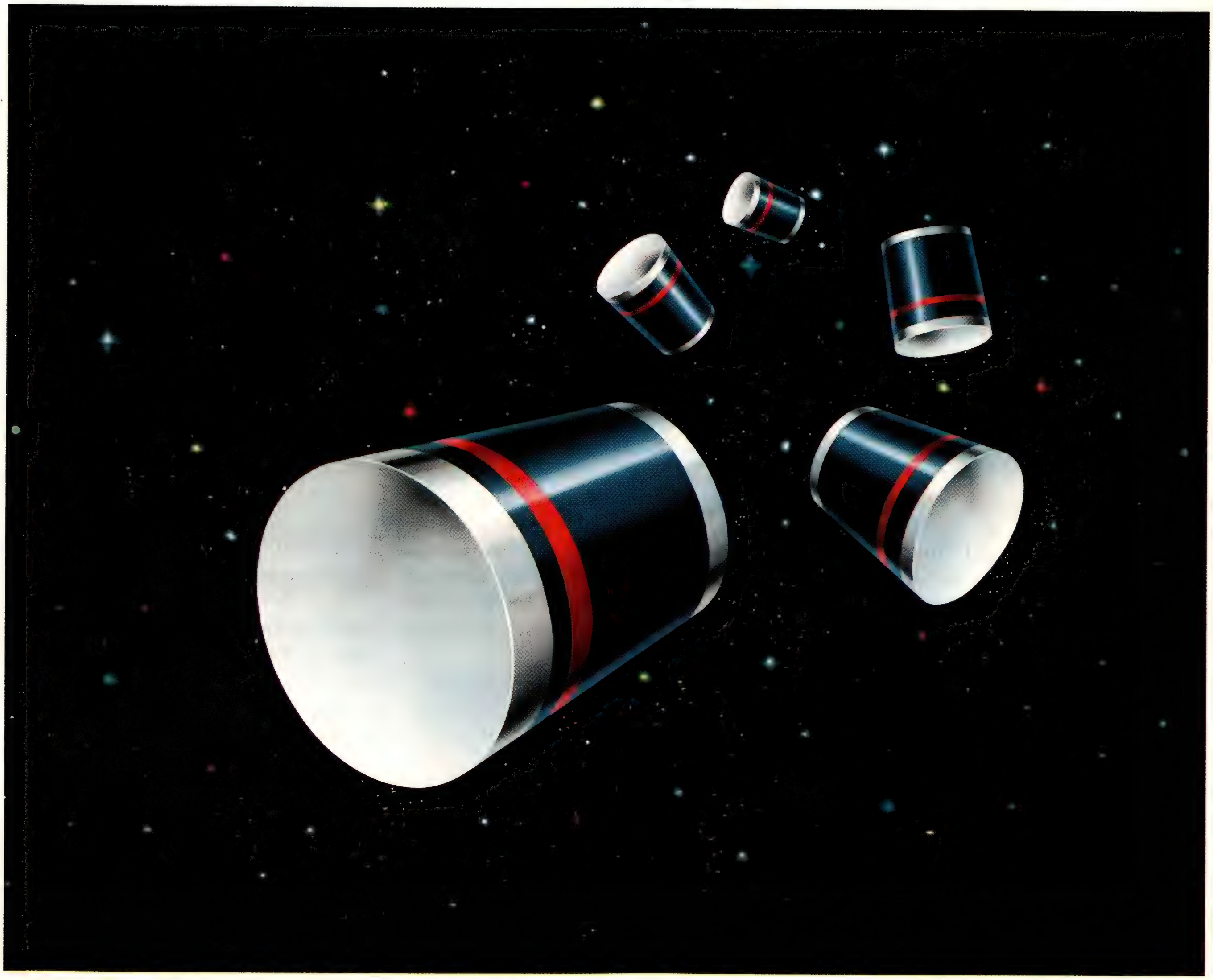

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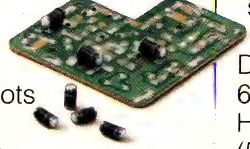

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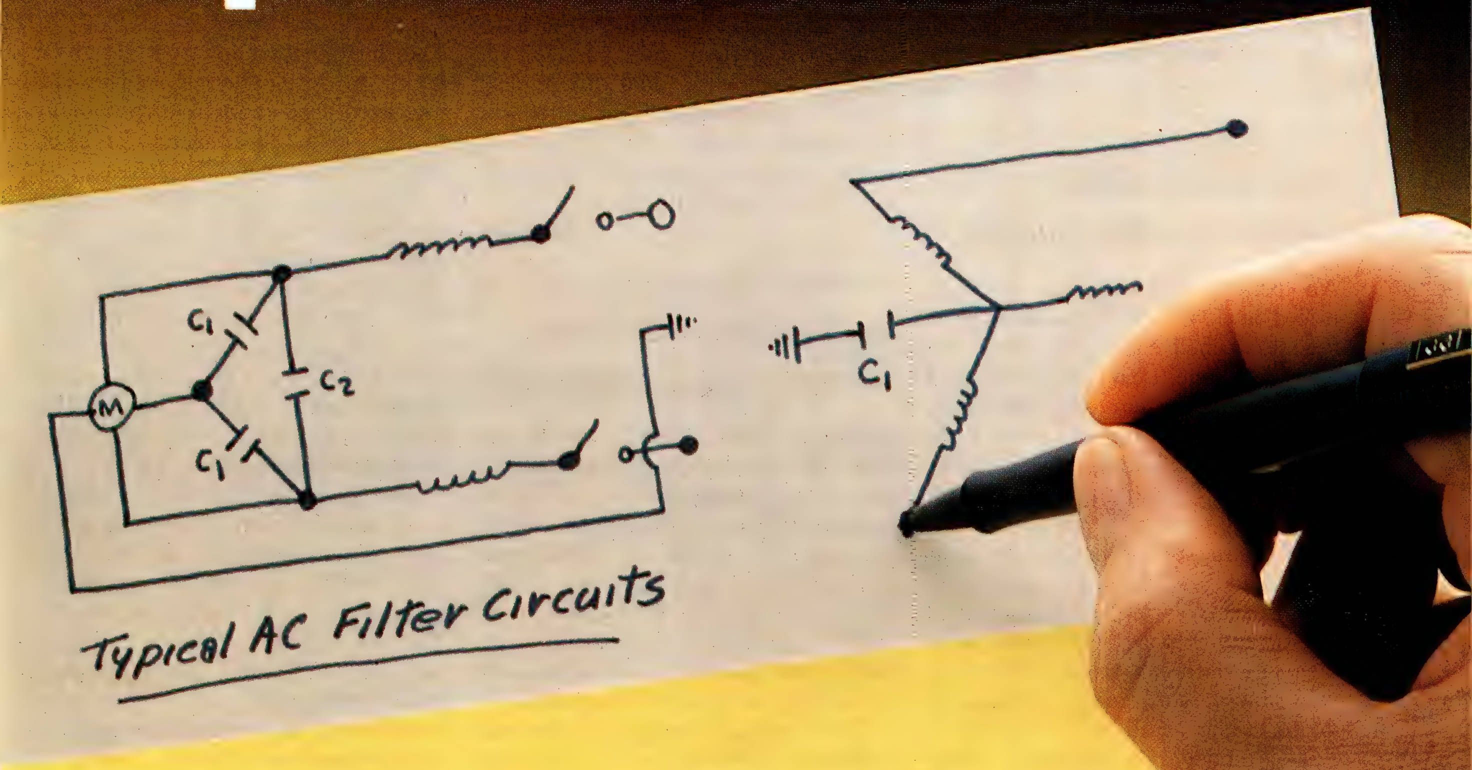
Tradeoffs in capacitor selection



There's no tradeoff for safety.

Shock protection. Noise suppression. Reliable shielding against input voltage spikes. There's no room for compromise if you want to protect your equipment and the people who operate it.

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TRW's AC-rated capacitors make the choice easy . . . because they're rated up to 460 VAC. The metallized polyester dielectric makes them physically small, yet offers long life without the use of impregnants. And the flame-retardant polyester tape-wrap case and epoxy end-fill protect the dielectric against heat, cold, moisture and physical shock. There's never a question about safety.

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AC Voltage Rating	330	370	460	200
Dielectric Strength VDC	900	1500	2100	400
Max. Corona-Free VRMS	412	460	600	290

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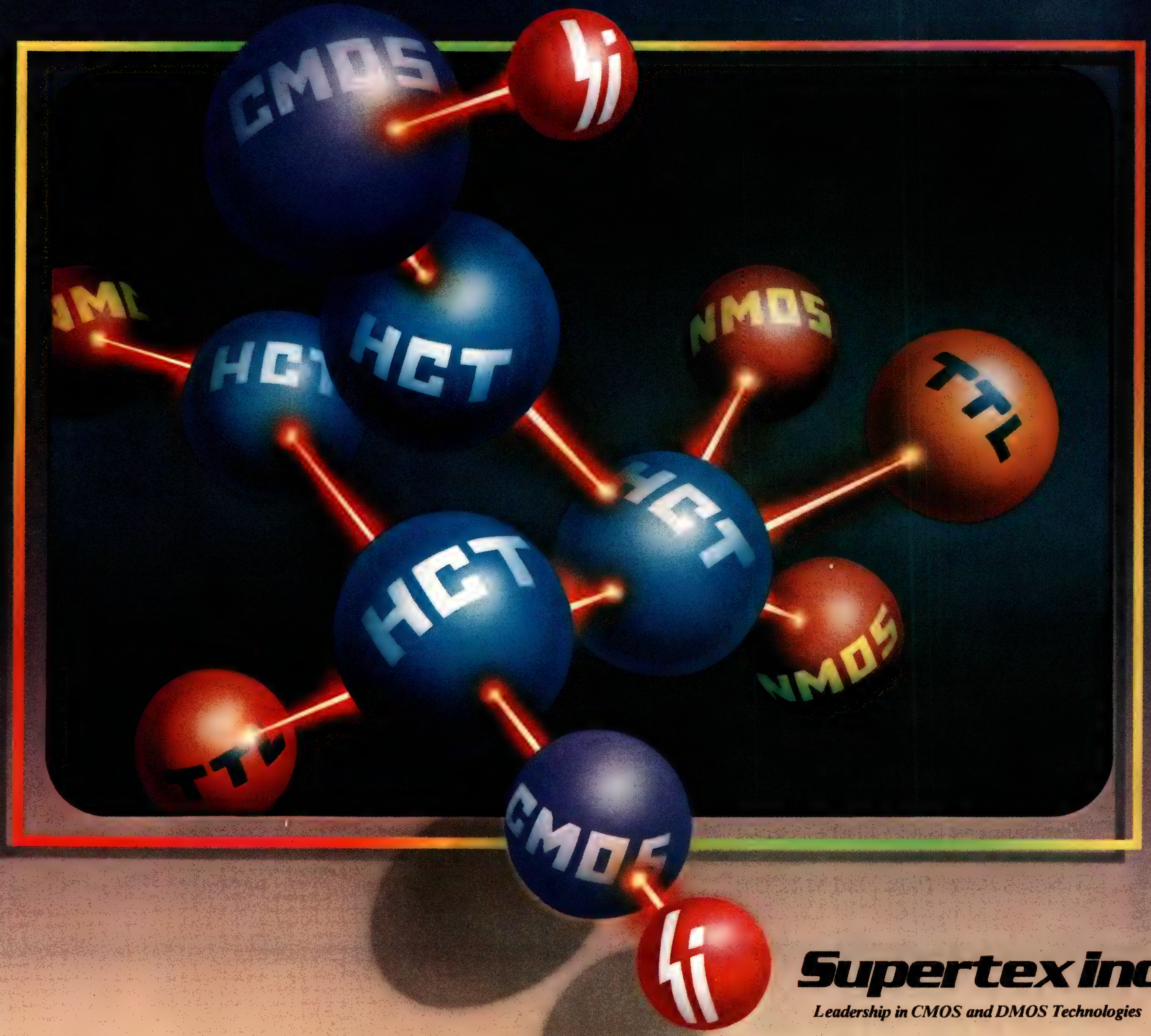

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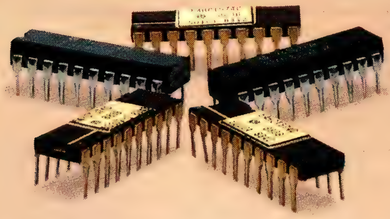

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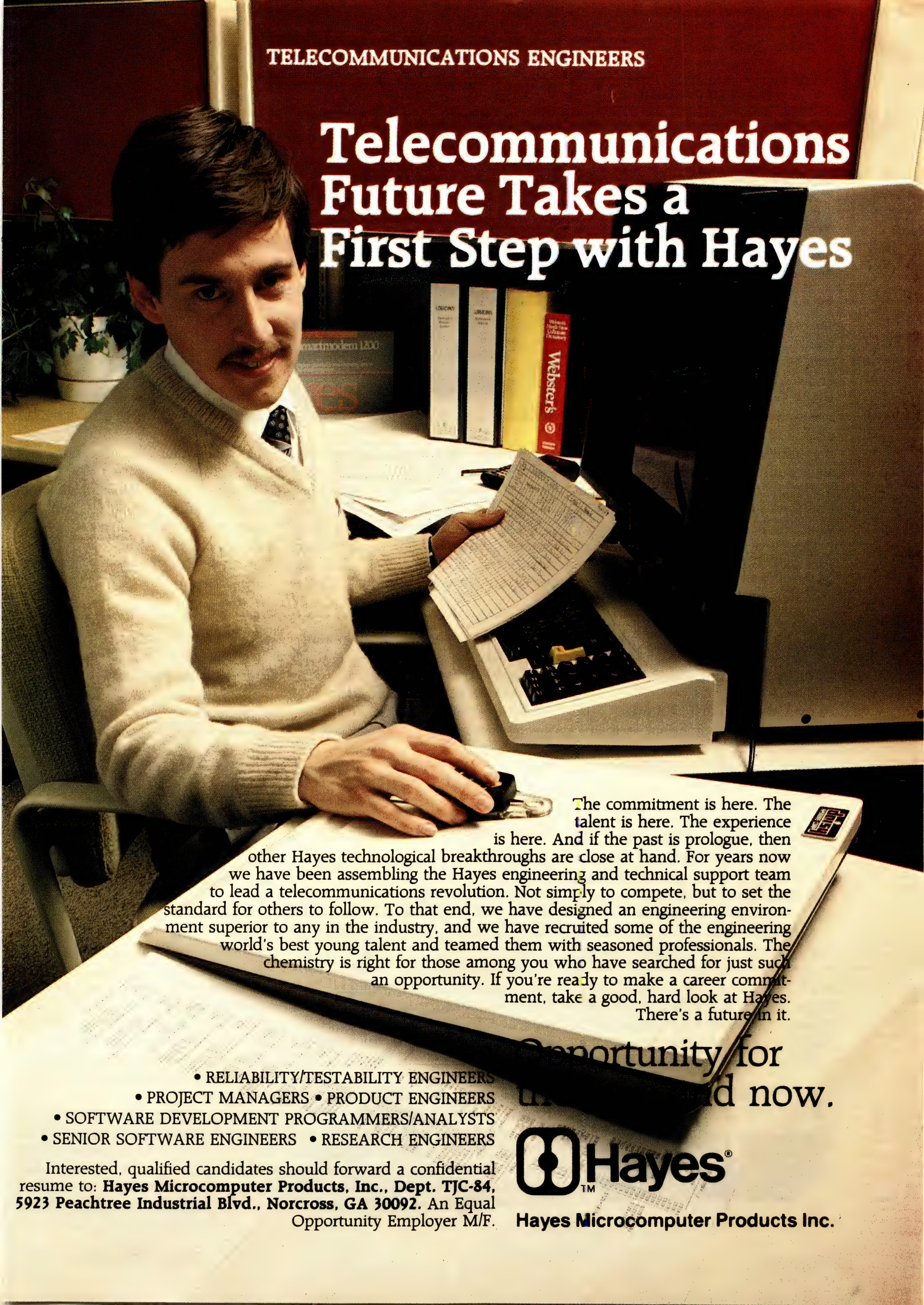

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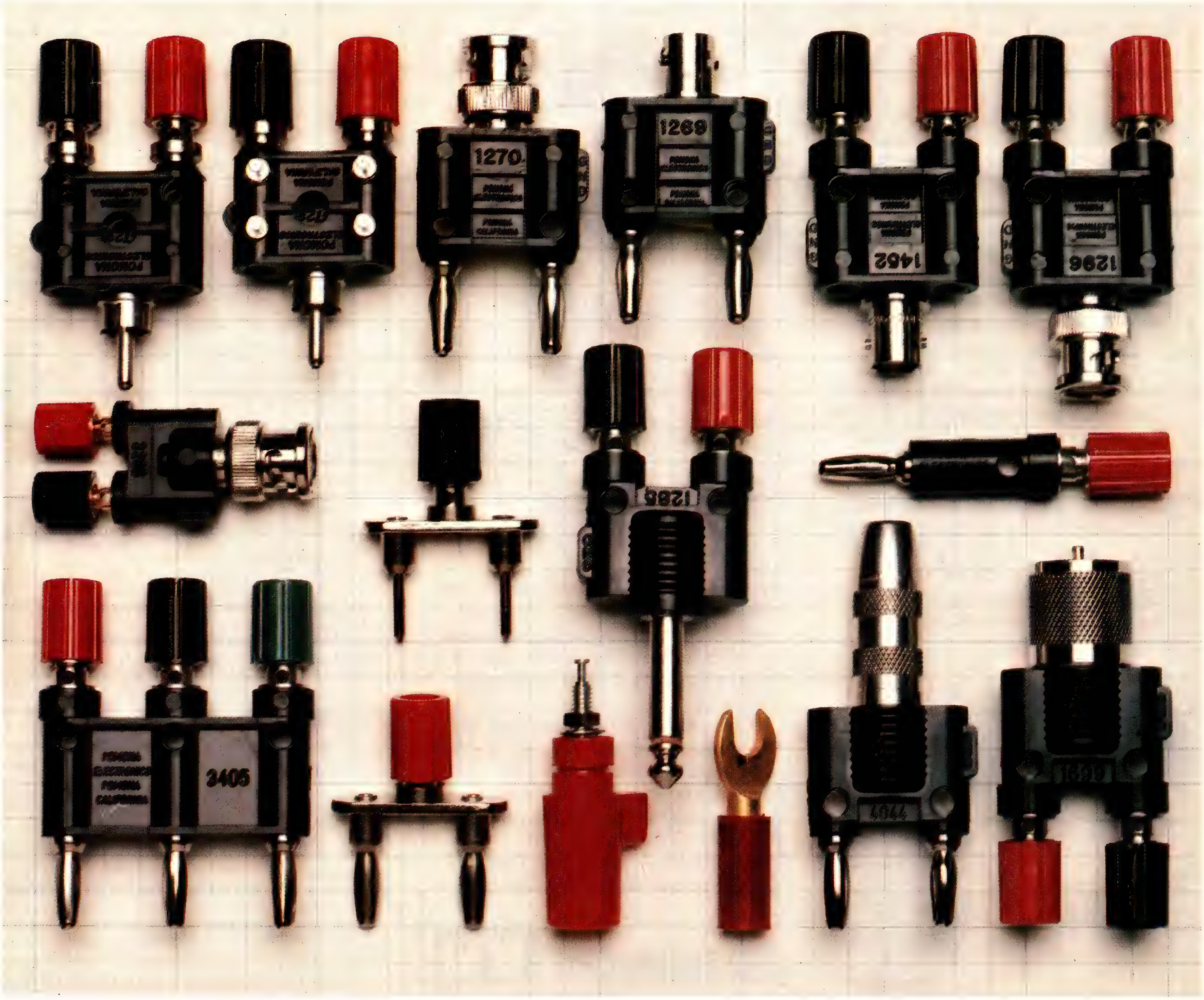

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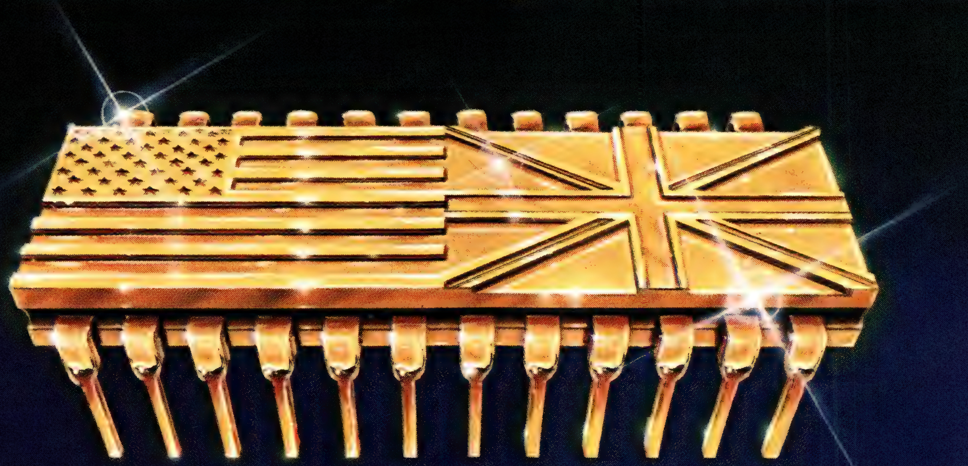

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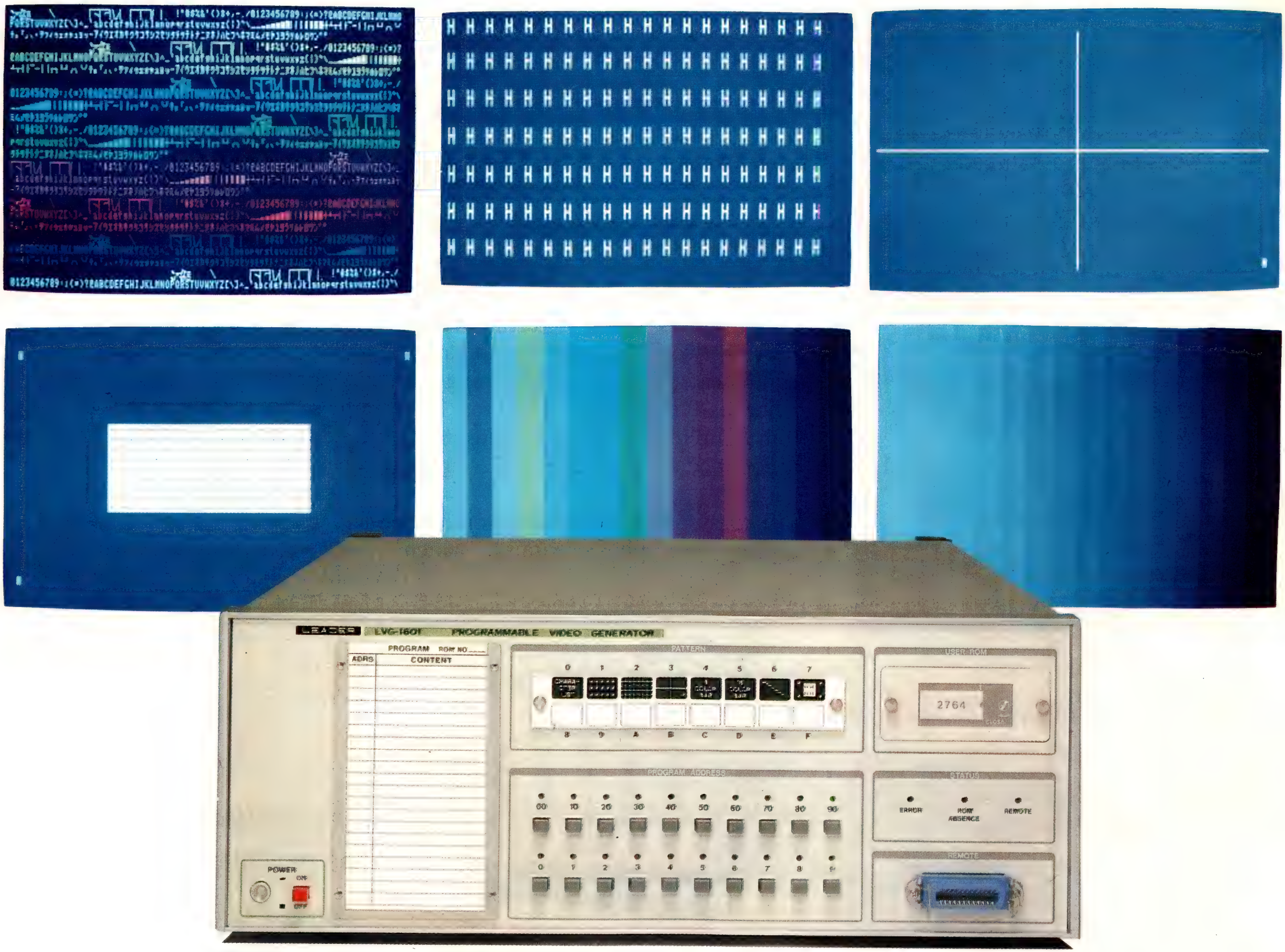

PROGRAMMABLE VIDEO GENERATOR
NEW LVG-1601

Remote control connector

FOR THE ATTENTION OF PRODUCTION/ SERVICE MANAGERS OF CRT DISPLAYS

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Automation is increasingly the key to productivity and improved quality in industry. So it's hardly surprising that the market for factory automation is growing at over 25% a year, even in the teeth of world recession.

And when you think of factory automation, you're almost certain to think of Gould – a world electronics leader, and a major and growing producer in Europe. Several divisions combine to produce totally integrated systems – including the world's first programmable controller with the speed and precision needed to handle servo-drives.

Gould is concentrating its resources on six key areas: high-performance 32-bit minicomputers, factory automation, test and measurement, medical electronics, defence electronics and electronics components and materials. All are growth areas of increasing importance to Europe – so the Gould commitment to doubling manufacturing and sales in Europe over the next few years makes good sense, both for Gould and its customers.

If you'd like to know more about our company, our growth strategy and our products, write to Gould, Department V5, Raynham Road, Bishop's Stortford, Hertfordshire CM23 5PF, England.

GOULD
Electronics

Circle 222 on reader service card

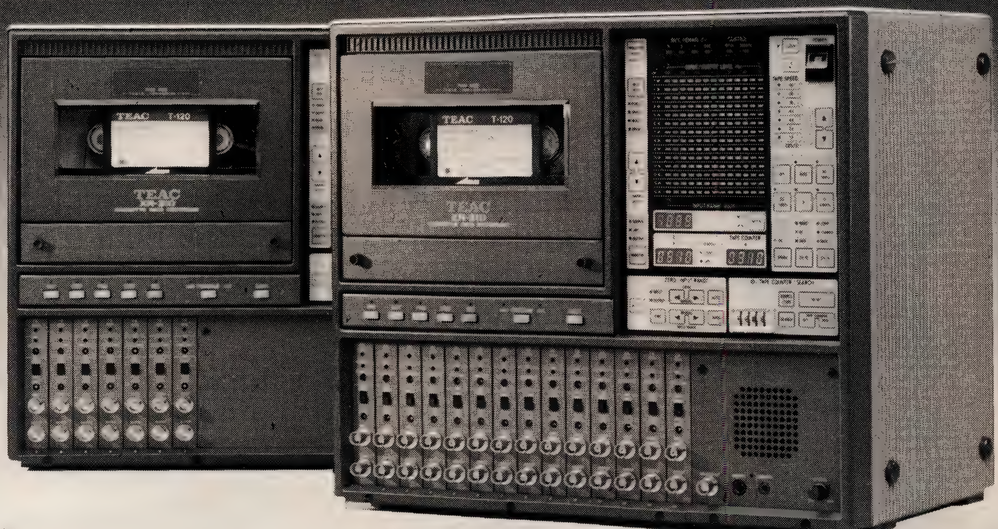
TEAC Puts More Versatility in Data Recording

XR-310
XR-510

Videocassette format with extensive microcomputer control.

The XR-310 and XR-510 data recorders offer 7 and 14 data tracks plus a memo announce channel, respectively, on 1/2-inch videocassette tape. Thanks to extensive computer control, they provide high quality performance and unmatched operation ease. Compatibility with the XR-30 and XR-50 gives you greater system flexibility.

■Computer control using three microprocessors. ■Auto Program Loading function sets pre-record conditions. ■Centralized control panel with flat-panel switches. ■One-touch Self-Check function. ■Bar-graph type LED level meters. ■Optional GP-IB interface.



XR-30/50/70

Multi-speed, multi-channel capability with easy portability.

These three portable data recorders provide the multitrack capabilities and performance of open reel recorders with the convenience of cassette recorders. They have four selectable speeds with 8, 15, and 22 channels, respectively, and use 1/2-inch videocassette tape.

■Wide-bandwidth FM recording system standard, DR option available on XR-30 and XR-50. ■Two-way (AC/DC) power supply capability with optional DC power supply unit. ■Independent rec/reproduce heads for tape/source monitoring. ■Tape servo and noise compensation channels.

TEAC

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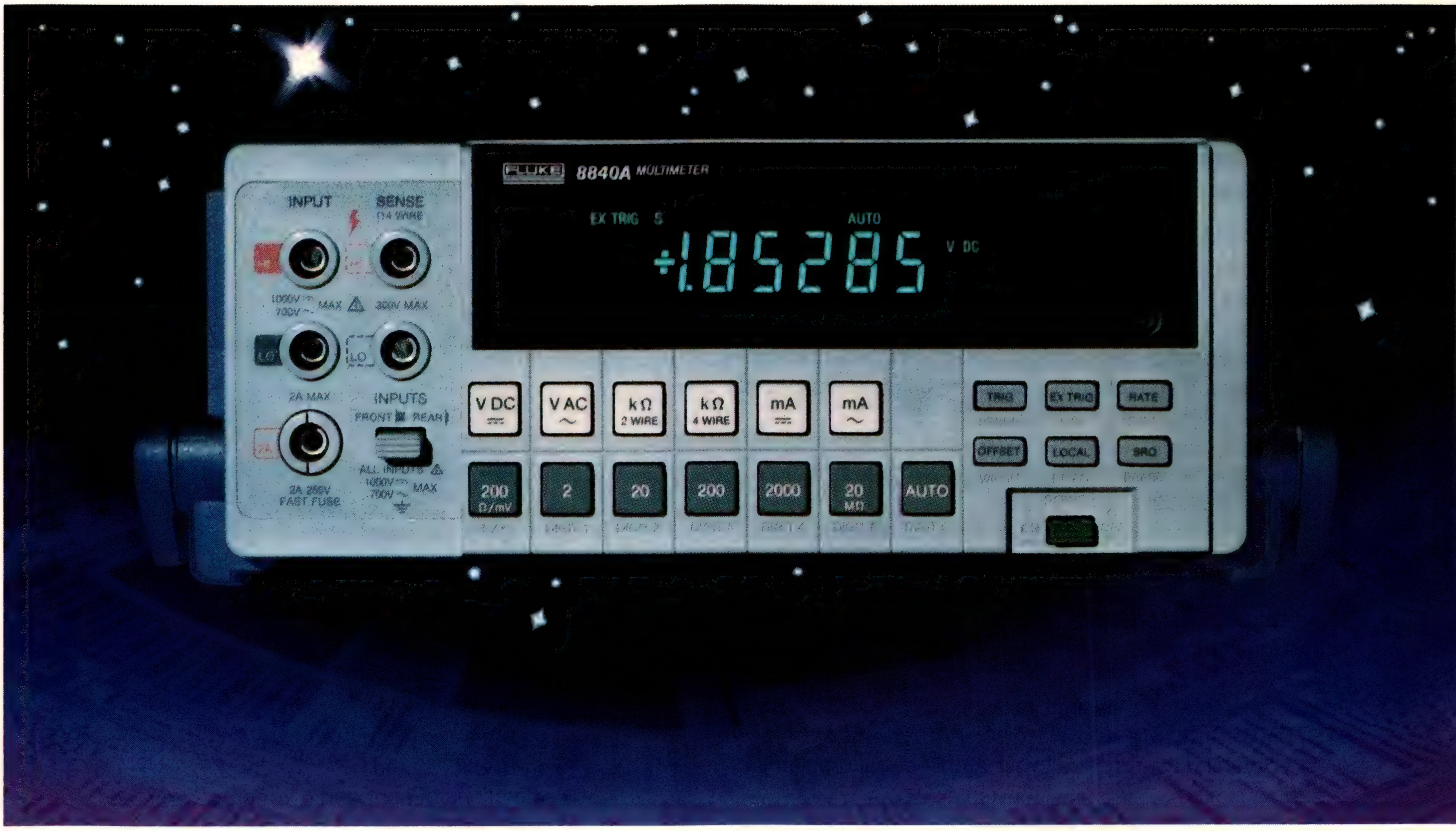
IEEE-488

A clear display of superior performance.



Introducing the Fluke 8840A Digital Multimeter

One look tells you it's different.

From its exclusive vacuum fluorescent display that's easier to read. To a simplified new design that's easy to use.

But look again.

Because inside are more features for less money than any other 5½-digit DMM in its class.

Including superior dc accuracy that the competition can't touch— 50 ppm for 1 year; 20 ppm for 24 hours.

There's closed-case calibration. And two self-test levels are built in to ensure accuracy and ease of service.

The 8840A comes standard with dc volts, 2- and 4-wire ohms, current and sensed front/rear input switching.

It has fast autoranging and multiple reading rates. Plus you can add two inexpensive options: IEEE-488 and true rms ac.

You can't see them, but the 8840A is filled with new Fluke manufactured ICs and devices for even greater accuracy and reliability.

But there is one thing you **can** see that automatically makes the new Fluke 8840A today's best buy in a bench or rack-mounted DMM.

Its price. $695.*

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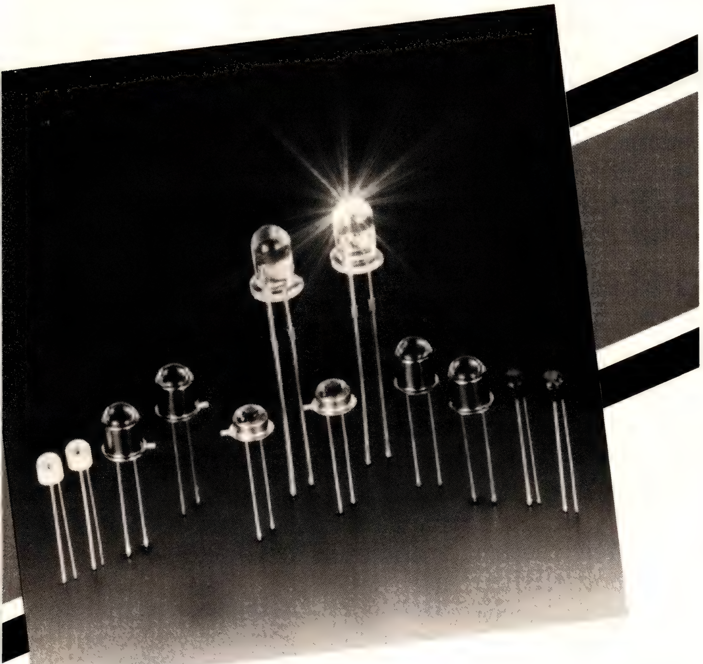
I.M.T., the new high technology company in optical semiconductors, I.M.T. Has Emerged

The Origin of a Technology-Development Company in Optics

May 1984-- a new, high-technology enterprise is formed in Japan.
Its name is **International Micro Technology** (I.M.T.).
The name I.M.T. was chosen for the enterprise to indicate the promotion and development of an international information society, to meet the needs of people all over the world. We will contribute to this future society by developing new optical technology and exploring new areas of technology.



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A center for development and production is under construction in the Japan Alps, at the center of precision engineering technology.
We are striving for production in line with our theme-- *contribution to people* --in an advanced enterprise that is in harmony with nature.

To Build The 21st Century with You

Our company has been established as a leader of these industries with ample high technology toward the 21st Century.
We are developing a world-wide activity.
We want to build the society of the 21st Century with you.

Products

Optical Semiconductors =Light-emitting diodes. Photo diodes, Photo transistors, Optical ICs, Optical sensors
Lasers=Digital audio disks, Optical fiber communication, Laser beam printers, Sensors, Computer terminal data transmitters, Optical disk memories
CCD=Image pickup devices, Memories, Analog signal-processing devices

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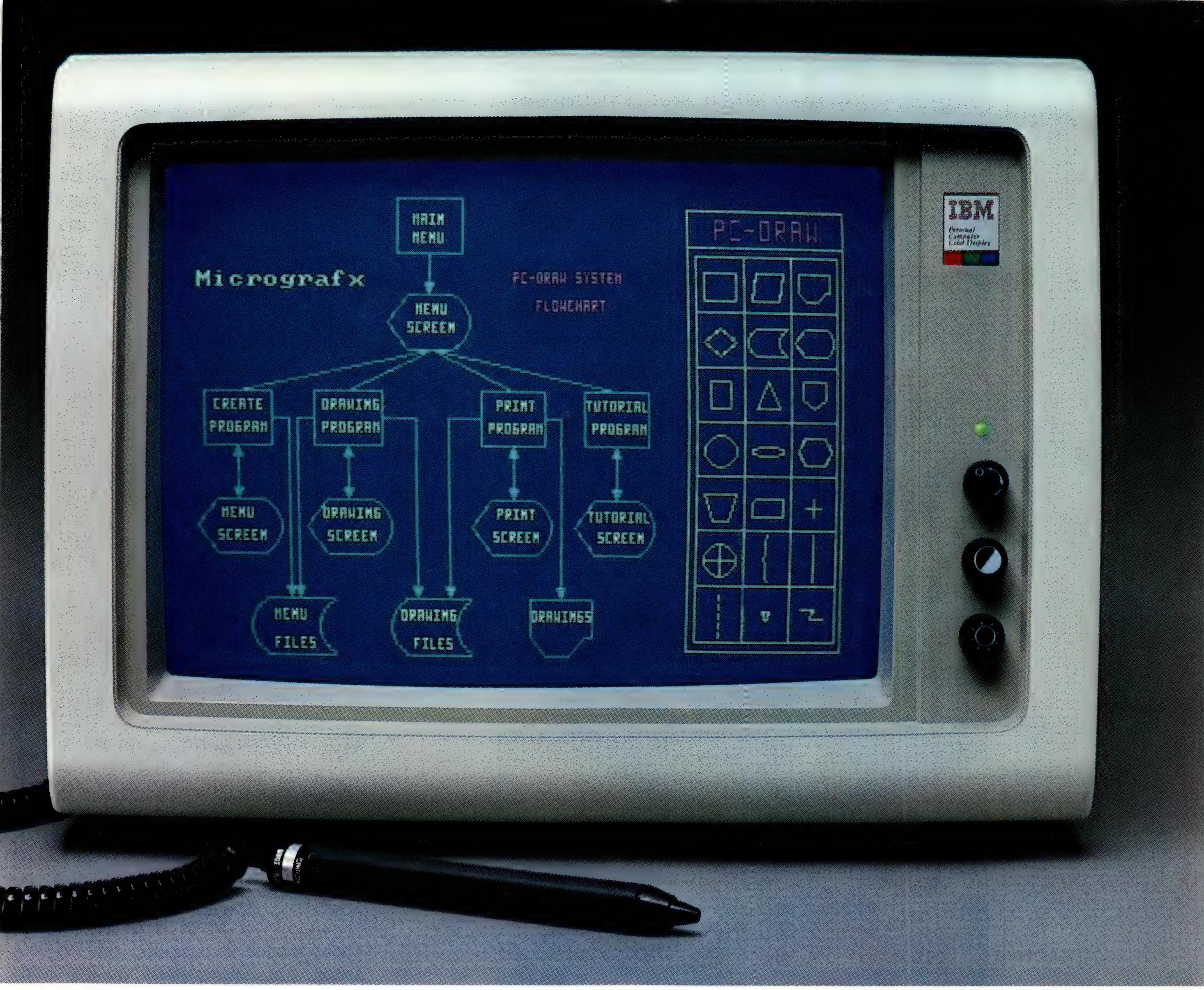
Circle 197 on reader service card



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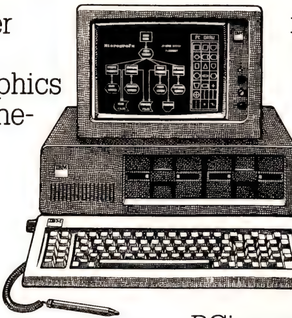

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Circle 199 on reader service card

The first 10 MHz monolithic FIR filter

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- **FIR "Building Block"**
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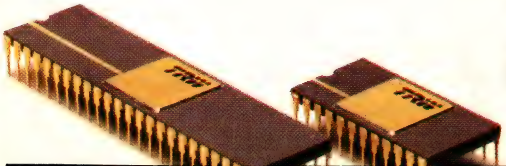

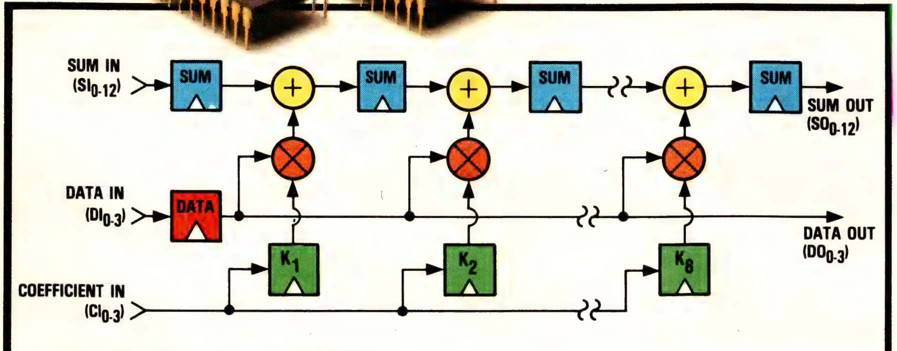

Simplified Block Diagram TDC1028

Now available from TRW—the first and only high-speed monolithic FIR digital filter! Our new TDC1028 4-bit FIR digital filter is a bit-slice "building block" cascadable to more than 36 stages without external components.

Key features include independently expandable coefficient or signal word size, and independently selectable format for coefficients and signal data words. *And—no other monolithic device can provide such precise filtering at such high speed—10 MHz throughput rate!*

The companion TDC1011 8-bit shift register provides easy word-size expansion of the TDC1028. The shift register can be programmed to any length between 3 and 18 stages, and operates at a 20 MHz rate. *And—it's the only variable length shift register available today!*

Both our TDC1028 and TDC1011 are fully TTL compatible and operate from a single +5V power supply. The TDC1028 is available in a 48 lead DIP, and leaded or contact chip carrier; the TDC1011 comes in a 24 lead DIP, or CERDIP.

The high-speed FIR digital filter and shift register may be used in such applications as telecom, sonar, radar, medical, computer graphics, TV special effects, etc.

The U.S. price in 1000s for the TDC1028 is $59 (commercial DIP); the TDC1011 is $23 (commercial CERDIP). Both are available now from Arrow Electronics, Hall-Mark or Hamilton/Avnet. For data sheets and application notes, circle reader service card. Or, for super fast information, call or write our Literature Service Department:

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TRW Electronic Components Group,
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Circle 201 on reader service card

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Circle 203 on reader service card

pacitors and hermetically sealed switching transistors. All models have ⅛-in.-thick aluminum sheet casings.

The switchers are priced at $221 and up in large quantities and are available from stock.

Lambda Electronics, 515 Broad Hollow Rd., Melville, N. Y. 11747. Phone (516) 694-4200

[Circle 383]

Standby power systems put out 400 or 800 VA

A plug-in standby power source provides off-line battery/inverter backup power for protection against blackouts. Available in 400-VA and 800-VA output models, the portable SPS is designed for applications that do not require the continuous, clean power of an uninterruptible system. Typical applications include use with point-of-sale terminals, laboratory test gear, critical process controls, and communications equipment. Both the 400-VA and 800-VA units are available in models to handle 120-V, 60-Hz or 220/240-V, 50-Hz inputs.

The SPS operates by switching from line power to battery/inverter power within a half cycle when line voltage drops below a preset level. When the ac line voltage reaches –15% of nominal, the load is transferred to the inverter within 4 to 14 ms. When ac voltage returns to within 10% of nominal, the load is retransferred within 2 to 4 ms.

When the ac line is present, the SPS guards against transients and electrical noise in frequency ranges of 10 KHz and above; attenuation is rated at 40 dB minimum at 100 KHz. When supplying battery/inverter power, the SPS provides clean sine-wave output with voltage regulated to within 3% of nominal and total harmonic distortion limited to less than 5%.

The 400-VA model is priced at about $720, the 800-VA model at about $850. The products are available now.

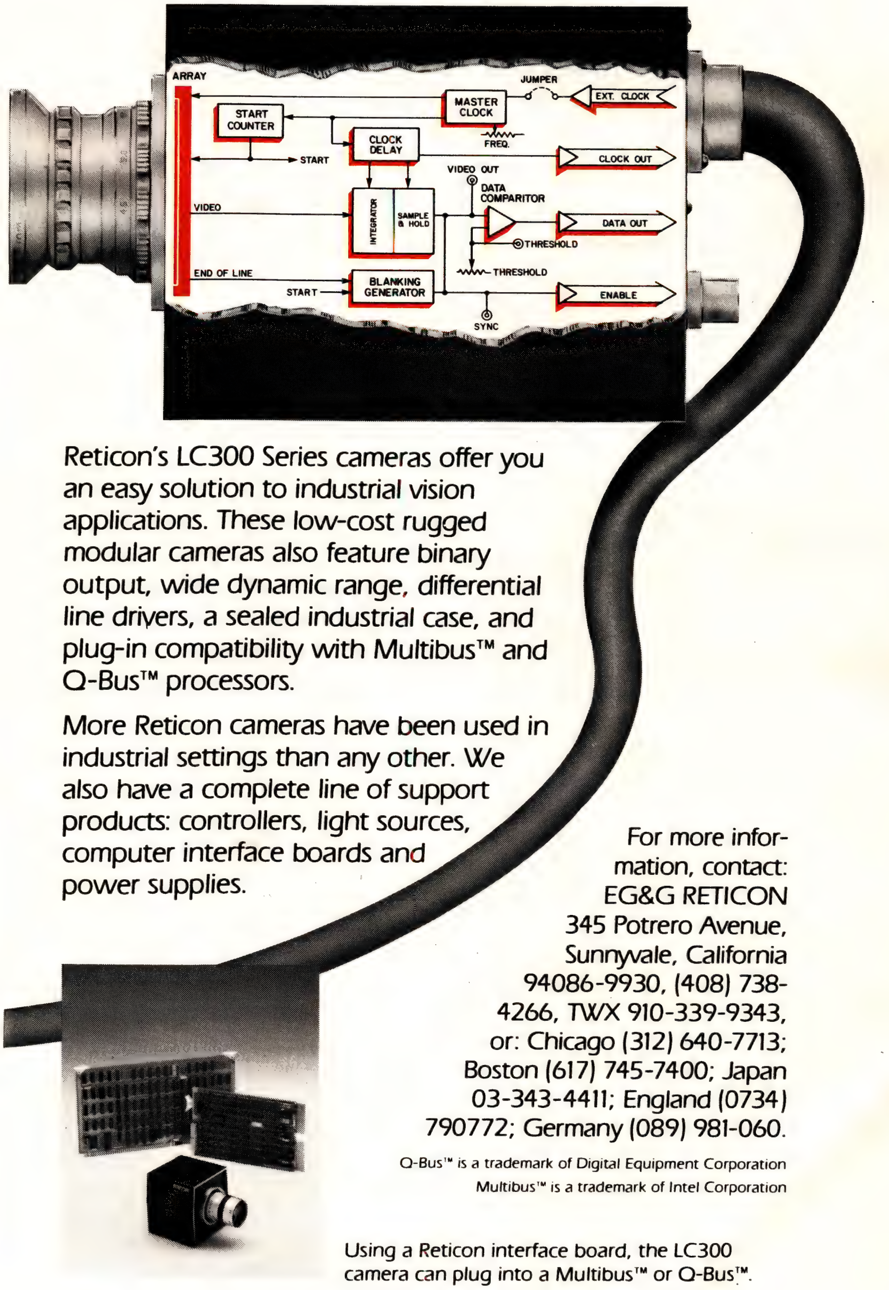
Sola Electric, 1717 Busse Rd., Elk Grove Village, Ill. 60007. Phone (312) 439-2800

[Circle 384]

Industrial Instrumentation Camera

AS SIMPLE AS 1,2,3

1. Internal clock
2. Single video line output
3. From $850 in single quantities



Reticon's LC300 Series cameras offer you an easy solution to industrial vision applications. These low-cost rugged modular cameras also feature binary output, wide dynamic range, differential line drivers, a sealed industrial case, and plug-in compatibility with Multibus™ and Q-Bus™ processors.

More Reticon cameras have been used in industrial settings than any other. We also have a complete line of support products: controllers, light sources, computer interface boards and power supplies.

For more information, contact:
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Q-Bus™ is a trademark of Digital Equipment Corporation
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Using a Reticon interface board, the LC300 camera can plug into a Multibus™ or Q-Bus™.

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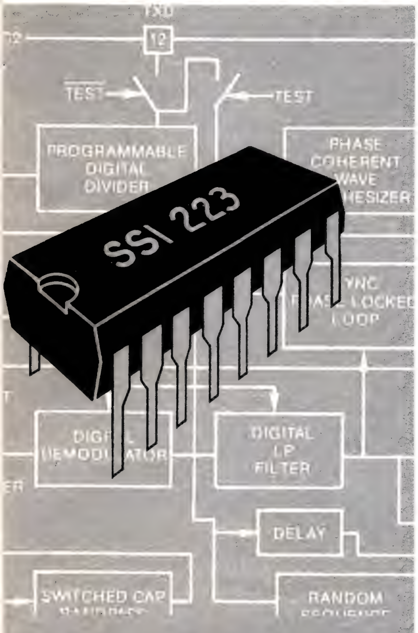
NEW LOW COST 1200 BAUD MODEM



Silicon Systems now introduces a low-cost 1200 baud FSK modem IC that is ideally suited for use with interactive terminals, videotex, personal computers, credit verification systems, point-of-sale terminals, and remote process control.

The new SSI 223 integrated circuit receives and transmits serial binary data over existing telephone networks using a frequency shift keying (FSK) design. It operates at 1200 baud and provides the filtering, modulation, and demodulation to implement a serial, asynchronous, data communication channel.

By utilizing advanced CMOS switched capacitor filter technology, Silicon Systems has been able to produce a chip that minimizes size and power consumption and maximizes reliability. Capable of simultaneous transmission and reception, the SSI 223 can be used for half-duplex operation over a single line system or full duplex operation over a two-line system.

For more information on this low-cost modem, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680, **(714) 731-7110,** Ext. 575.

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INNOVATORS IN INTEGRATION

Circle 207 on reader service card

Semiconductors

Static RAM boasts 35-ns access time

Manufactured in a complementary-MOS process using 2-μm geometries and 1.5-μm channel lengths, the IMS1423 4-K-by-4-bit static random-access memory achieves access times as low as 35 ns. The technology employed allows smaller memory-cell sizes than a comparable n-channel-MOS process, and it also results in 11-mm² die sizes. Power dissipation is as low as 500 mW when active and 85 mW when standing by.

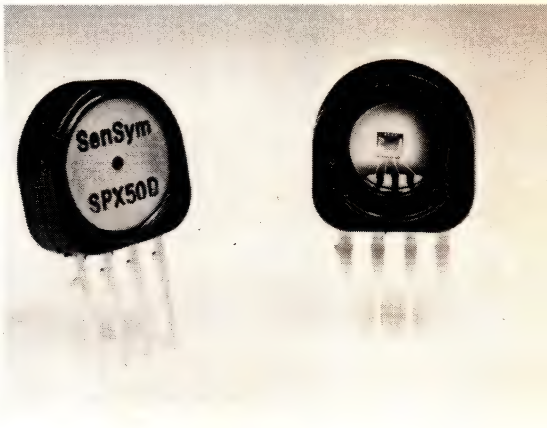
The IMS1423 initially will be offered with 35-, 45-, and 55-ns access times. In ceramic dual in-line packages, the parts sell for $64.50, $42.85, and $21.45 per unit, respectively, in lots of 100. Delivery takes six weeks.

Inmos Corp., P. O. Box 16000, Colorado Springs, Colo. 80935 Phone (303) 630-4453
[Circle reader service number 411]

Pressure sensor utilizes stress transducer technology

Available in two models, an integrated-circuit pressure sensor is designed for use in such areas as medical equipment and computer peripherals. The SPX50A/D piezoresistive sensors, one for absolute and the other for differential measurements, use an ion-implanted resistor in a silicon diaphragm to provide an electrical output proportional to applied pressure and related shear stress.

The ICs operate in the 0-to-50-kilopascal pressure range and have 0.1% full-scale combined linearity and hysteresis. The SPX50A has an integral vacuum reference and an output voltage proportional to absolute pressure. The SPX50D allows pressure to be applied to either side of the diaphragm and can be used for differential pressure measurements.



Priced at $26.50 each in sample quantities, both models are available now to original-equipment manufacturers. Volume quantities will be available in the third quarter for under $5 each.

Sensym Inc., 1225 Reamwood Ave., Sunnyvale, Calif. 94086. Phone (408) 744-1500
[Circle 416]

Power booster is designed for TV, monitor applications

The TDA8170 power booster is a monolithic integrated circuit designed to directly drive the vertical windings of cathode-ray-tube yokes. Housed in a high-power package called Heptawatt, the IC is used in vertical-deflection output in TV and monitor applications and provides efficient power amplification, flyback generation, reference voltage, and thermal protection.

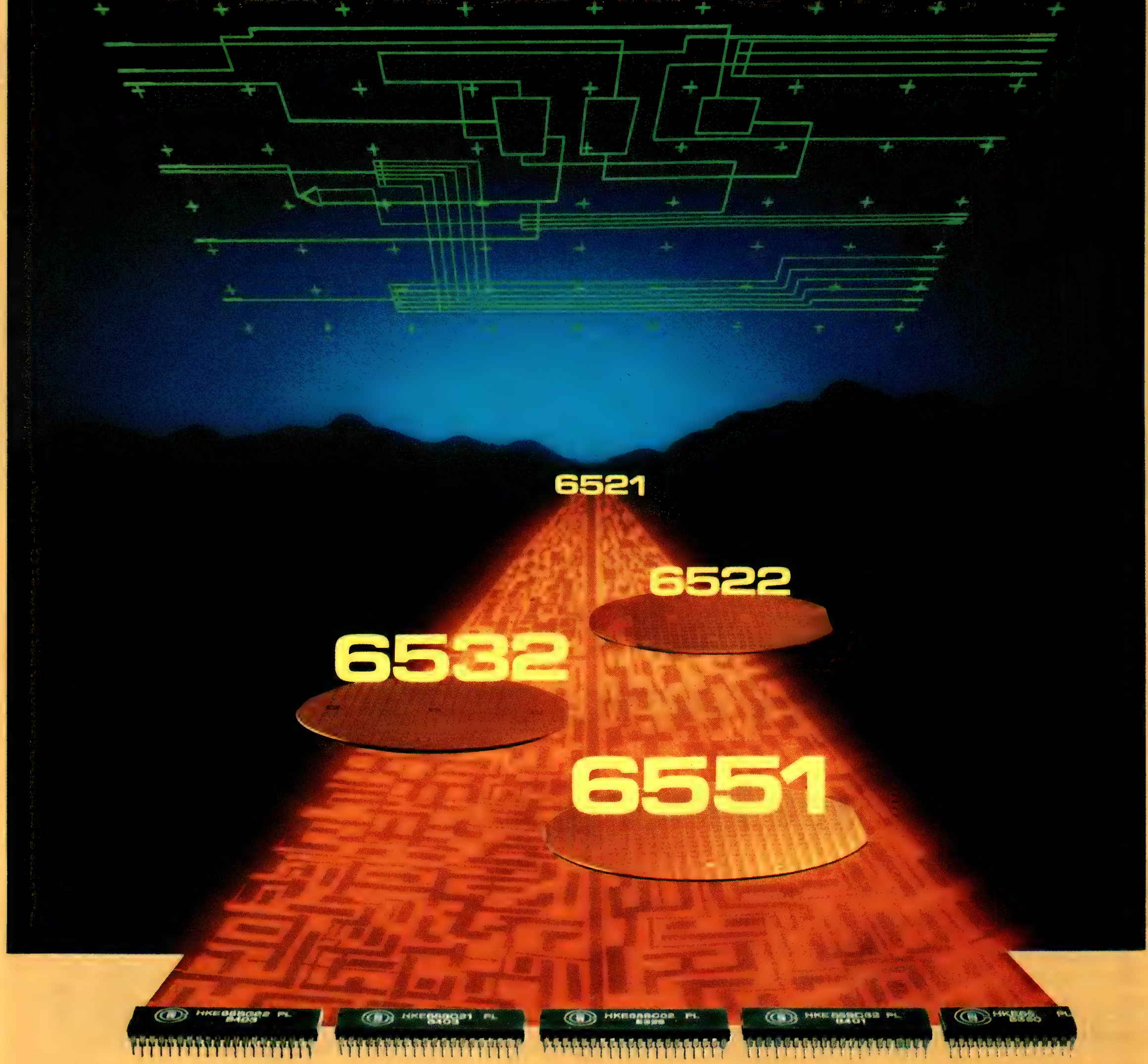
Priced at $2.36 per unit in quantities of 1,000 or more, the TDA8170 is available now.

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, Ariz. 85022. Phone (602) 867-6100
[Circle 414]

C-MOS driver ICs minimize MOS FETs' switching losses

Three complementary-MOS integrated circuits translate TTL or C-MOS low-level input signals into an output-voltage swing equal to that of the supply. The TSC426 has two inverting drivers, the TSC427 is noninverting, and the TSC428 is made from

CMOS 6502 MICROPROCESSOR THE HKE65SC02 FAMILY AND PERIPHERAL CHIPS



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Circle 209 on reader service card

Products newsletter

Half-height Winchester stores 100 megabytes

Advanced Storage Technology Inc., of San Jose, Calif., has produced a half-height 5¼-in. Winchester disk drive with a storage capacity of over 100 megabytes and average access times under 30 ms. Employing thin-film recording heads with a closed-loop servo system and plated media, **the model AST 96203 is formated with 960 tracks/in. and 20,880 bytes per track.** Another model, the AST 96202, has a capacity of 62 megabytes. Both models will be available in the fourth quarter in two formats—an entire disk drive or just the head-disk assembly. The drives will sell for about 25% less than full-height drives.

E-PROM programming cut to 10 ms

Thanks to design and processing enhancements, Texas Instruments Inc.'s erasable programmable read-only memories from can now be programmed 5 to 10 times faster. **The required typical programming pulse width has been reduced from 50 ms to 10 ms** in the Dallas firm's 16-K E-PROM TMS2516, 32-K E-PROM TMS2532/A, and 64-K E-PROM TMS2564 models. The E-PROMs, available now in dual in-line ceramic packages, have prices ranging from $6.68 for the TMS2516-35JL to $12.40 for the TMS2564-35JL in 100-piece lots.

Plug-in graphics board emulates Tektronix 4010

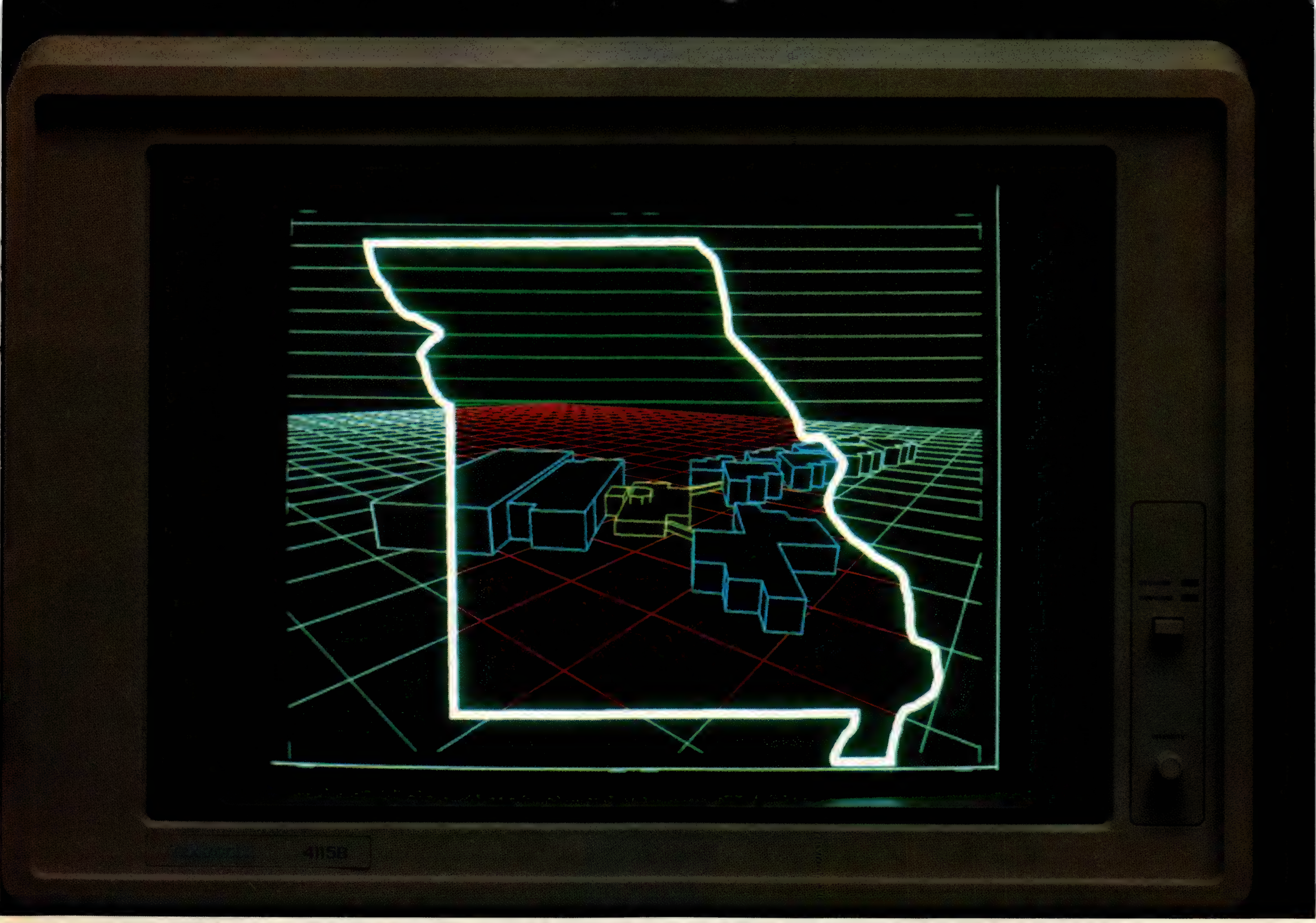
The SG240 graphics-enhancement board from Selanar Corp., of Santa Clara, Calif., features a resolution of 800 by 240 picture elements, noninterlaced. **The 4½-by-5-in. plug-in board also offers Tektronix 4010/4014 emulation,** 4,096-by-4,096-bit addressability, and Plot 10 compatibility. Available in 30 days, the boards sell for $795.

Pipelining hikes speed in cluster controller

Four-Phase Systems of Cupertino, Calif., has announced a new line of clustered-terminal processors, the series 5000, which operates four times as fast as the series 4000. **The boost in speed comes from a hardware architecture based on pipeline processing,** which allows a number of distributed-information-processing functions to be performed simultaneously. Because of this architecture, moreover, the 5000 series can support up to 64 work stations and printers. The two models in the series—the 700 and 800—support a new line of intelligent work stations called the Fastrak series. The 5000 series comes in various configurations: the model 700, for instance, with 33 work stations, a 1.5-megabyte memory, two 138-megabyte disk drives, a 600-line/min. printer, and ten 35-characters/s printers, sells for $214,373.

Probe lets logic analyzers capture random pulses

A low-cost glitch latching probe expands the capabilities of Racal-Dana Instruments Inc.'s series 200 logic analyzers by allowing the analyzers to capture random logic pulses, which may occur between clock edges. The Irvine, Calif., company's probe, designated Option 92, **provides four channels of both glitch detection and logic analysis and records logic glitches down to 10 ns.** The glitch channels also display on a cathode-ray tube the transitions occurring more than once through a predetermined voltage threshold within a single clock period. The probe is suitable for use with all common logic families and bus interfaces. Option 92 sells for $695 and is available in six weeks.



The St. Louis campus of McDonnell Douglas Automation Company as modeled by McAuto's Building Design System.

McAuto is building dreams in Missouri.

Learn how Missouri's new Customized Training Programs can cover up to 100% of all workers' expenses paid while in training. For details, call Governor Kit Bond, Sales Manager, Missouri Worldwide, 314/751-2939. Or write Box 118B, Jefferson City, Missouri 65102.

Every day, dreams become reality at McAuto, the worldwide computer services division of McDonnell Douglas Corporation. Here, a special combination of innovative ideas and technological advances is helping to shape our future. Buildings, machinery, and even jogging shoes are designed, tested and analyzed not on drawing boards, but on computer systems designed by McAuto. And it all takes place here in Missouri.

Bob Fischer, president of McAuto says, "People are our most vital resource. We've had great success in attracting and keeping the high quality work force our business demands. Our average employee has been with McAuto for eight years, a figure far above the industry average. Many come from colleges and universities located throughout the state. Others relocate here and find they like McAuto's atmosphere and they like living in St. Louis."

If you need a quality work force to turn your high tech dreams into reality, you belong in Missouri.
The Profit Center.

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Circle 213 on reader service card

Home Electronics Marketing

National revitalizes the home information systems revolution!

A new team is beginning to take shape at National Semiconductor's headquarters in Santa Clara, California. Its mission: to focus National's vast technological resources on home information systems.

Our start-up team will work with diverse systems and semiconductor technologies and disciplines to create and market breakthrough products. It could be the opportunity of the decade for top professionals in these areas:

Senior Systems Engineers Consumer TV Related Products

Role:

- Develop Viewdata/Teletext, digital TV type systems using advanced television sub-system partitioning, digital signal processing techniques, etc.
- Develop proof-of-concept prototypes
- Creative systems partitioning for linear and digital semiconductor integration
- Generate detailed specifications and documentation
- Work closely with marketing and IC design groups

Key Requirements:

- Proven industry experience in circuit systems hardware and software design
- Extensive knowledge of basic television engineering fundamentals
- Design experience in one or more of the following disciplines:
  Digital signal processing
  Teletext/Viewdata information systems
  Videographics/microprocessor systems communications
- Good communication skills
- Enthusiasm for the new and innovative
- 5 years of related experience
- BSEE or equivalent

Market Development Engineer Digital Consumer Electronics

Role:

- Development of advanced videographics and computer architectures for integrated circuits targeted at consumer electronics products
- Responsible for understanding product trends in the consumer market and the system performance trade-offs
- Screen and prioritize business opportunities
- Generates customer proposals aimed at promoting present products and identification of new dedicated systems products
- Responsible for new IC product recommendations

Key Requirements:

- Strong end user and design experience in digital consumer electronics
- Excellent technical and communication skills
- Good business sense and market trend knowledge
- 5 years of related experience
- BSEE and MBA desirable

Senior Systems Engineer Home Computer Products

Role:

- Develop advanced microcomputers systems and peripheral I/O devices based on new 8, 16 and 32 bit bus architectures
- Development of advanced videographics systems and LCD display systems
- Develop proof-of-concept prototypes
- Generate detailed specifications and documentation
- Work closely with marketing and IC design groups

Key Requirements:

- Proven industry experience in microcomputer systems hardware and software design
- Extensive knowledge of present microprocessor architectures and cost/performance trade-offs
- Systems knowledge of systems I/O devices, hard and soft disc, printers, modems, etc.
- Knowledge of semiconductor technologies and limitations
- Good communication skills
- Enthusiasm for the new and innovative
- 5 years of related experience
- BSEE or equivalent

Senior Systems Engineer Home Communications Products

Role:

- Develop advanced home communications products for voice and data distribution
- Develop proof-of-concept prototypes
- Generate detailed specifications and documentation
- Work closely with IC design groups and marketing personnnel

Key Requirements:

- Extensive experience in analog and digital communications systems. Phone line, coaxial links, fibre optics, and infrared remote controls and power line communications, etc.
- Knowledge of small area networks an advantage
- Good understanding of systems partitioning and trade-offs
- Knowledge of various semiconductor technologies and limitations
- Good communication skills
- 5 years or more of related experience
- BSEE or equivalent

For immediate consideration, send your resume to National Semiconductor, Dept. MS-SK, Professional Employment, P.O. Box 62499, Sunnyvale, CA 94088. Or call (408) 721-5866 from 9 AM to noon P.D.T. Or TWX 910-339-9240. We are an equal opportunity employer m/f/h/v.

Let's talk about your career.

National Semiconductor

Fairchild offers you a high-growth environment. (Literally).

Our new state-of-the-art art semiconductor facility in Puyallup (Pew-allop), Washington, is surrounded by a thick forest of towering fir and pine trees that average over 100 feet in height.

The recently-completed world-class facility is located in a campus-like setting just 10 minutes from Tacoma. The area is blanketed with the lush, green woods that typify the Pacific Northwest. Not so typical in the area is the multi-million dollar investment Fairchild has made to semiconductor technology for bipolar and MOS VLSI products. In fact, its full computer control design; high volume wafer starts per week capacity; and two micron capability would be exceptional anywhere. But together with the diverse cultural and recreational activities of the Seattle-Tacoma area, our new facility offers you a once-in-a-lifetime career opportunity.

If you're an experienced marketing, materials, engineering, or operations professional attracted by the high-growth environment of our new facility in Washington, then consider these chances to join us.

Marketing

Product Marketing Managers
Product Marketing Engineers
Business Planners

Materials

Production Control Managers
Product Planners
Senior Buyers

Engineering

Management and Engineering openings exist in the following areas:

Process Development
Product
Test
R&QA
Electronic Technicians
Product Development Technicians

Operations

Production Supervisors
Process Engineers
Equipment Engineers
Software/Hardware Engineers
Production Control Planners
Equipment Maintenance Technicians

We currently have openings ranging from SENIOR TO ENTRY LEVEL, including opportunities for recent college graduates in all of these areas. All of these openings require recent semiconductor experience, with at least a four year technical degree necessary to qualify for the professional opportunities.

Opportunities like these don't come around every day. Especially opportunities to combine technological growth with the natural beauty that the Puget Sound provides.

Apply by sending us your resume: Fairchild Memory and High Speed Logic Division, Dept. EM-614, 33309A First Avenue South, Federal Way, WA 98063-9701, Attn: Employment Office.

As an affirmative action employer, we encourage women, members of minority groups and the disabled to apply.

Memory and
High Speed Logic Division

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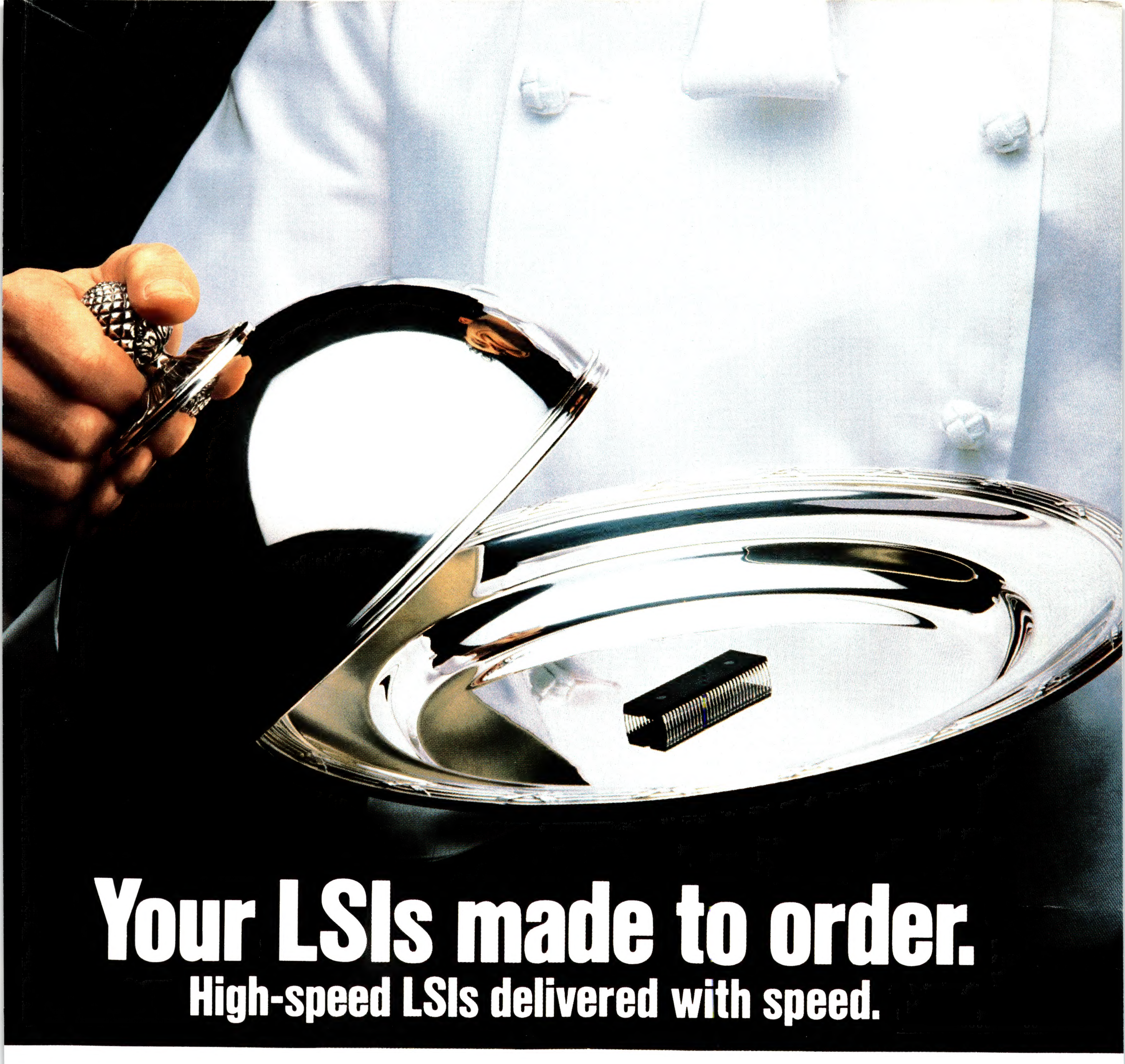
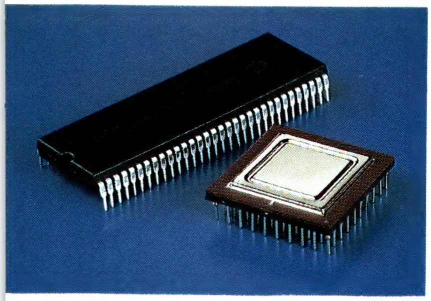


Your LSIs made to order.

High-speed LSIs delivered with speed.



What we offer are semi-custom LSIs with basic structures that are custom finished to match your logic circuits.

They can be ready soon after you order at an economical cost.

These are the high-speed, 2.5n sec., TC15G Series Gate Arrays and the ultrahigh-speed, 1.5n sec., TC17G Series Gate Arrays.

That's why Toshiba's world-leading CMOS and VLSI technology is appreciated around the world.

What's more, we have a wide line ranging from 880 to 10,000 gates. That means we have an LSI to meet any requirement.

Behind these LSIs is our superior CAD (Computer-Aided Design) system that supports designing these Gate Arrays.

Ask us. We will respond quickly and effectively to your requirements.

Toshiba CMOS Gate Array Series

	Series	High-speed Gate Array Series	Ultrahigh-speed Gate Array Series
Number of gates	880	TC15G008P (70)	TC17G008P (64)
	1,400	TC15G014P (88)	TC17G014P (82)
	2,200	TC15G022P (110)	TC17G022P (102)
	3,200	TC15G032P (134)	TC17G032P (124)
	4,200	TC15G042P (152)	TC17G042P (146)
	6,000	TC15G060P (176)	TC17G060P (182)
	8,000	–	TC17G080P (218)
	10,000	–	TC17G100P (228)

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